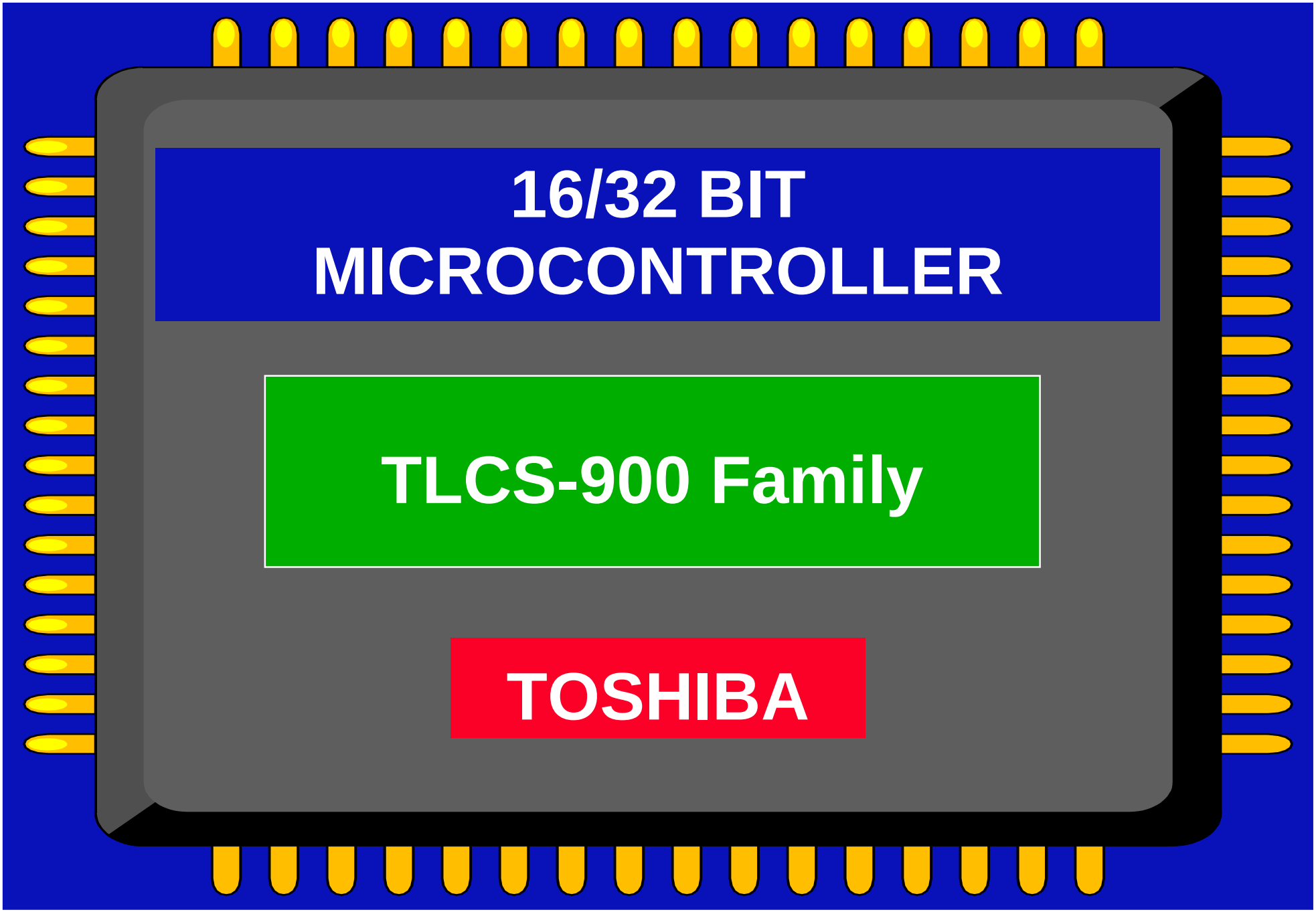
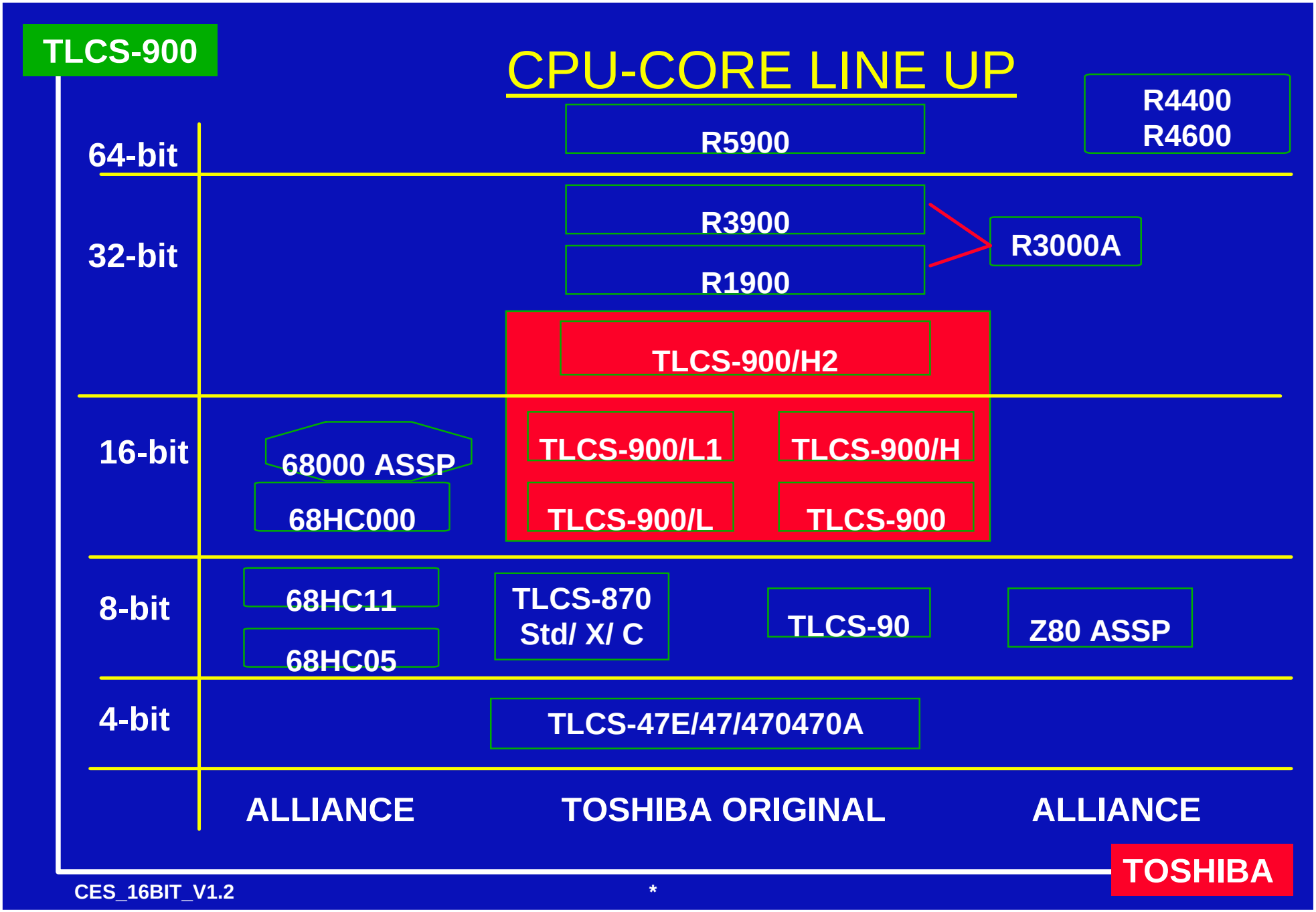

16/32 BIT
MICROCONTROLLER
TLCS-900 Family
TOSHIBA


TLCS-900
CPU-CORE LINE UP
R4400
R4600
64-bit
R5900
32-bit
R3900
R1900
R3000A
TLCS-900/H2
16-bit
68000 ASSP
68HC000
TLCS-900/L1
TLCS-900/H
TLCS-900/L
TLCS-900
8-bit
68HC11
68HC05
TLCS-870
Std/ X/ C
TLCS-90
Z80 ASSP
4-bit
TLCS-47E/47/470470A
ALLIANCE
TOSHIBA ORIGINAL
ALLIANCE
TOSHIBA

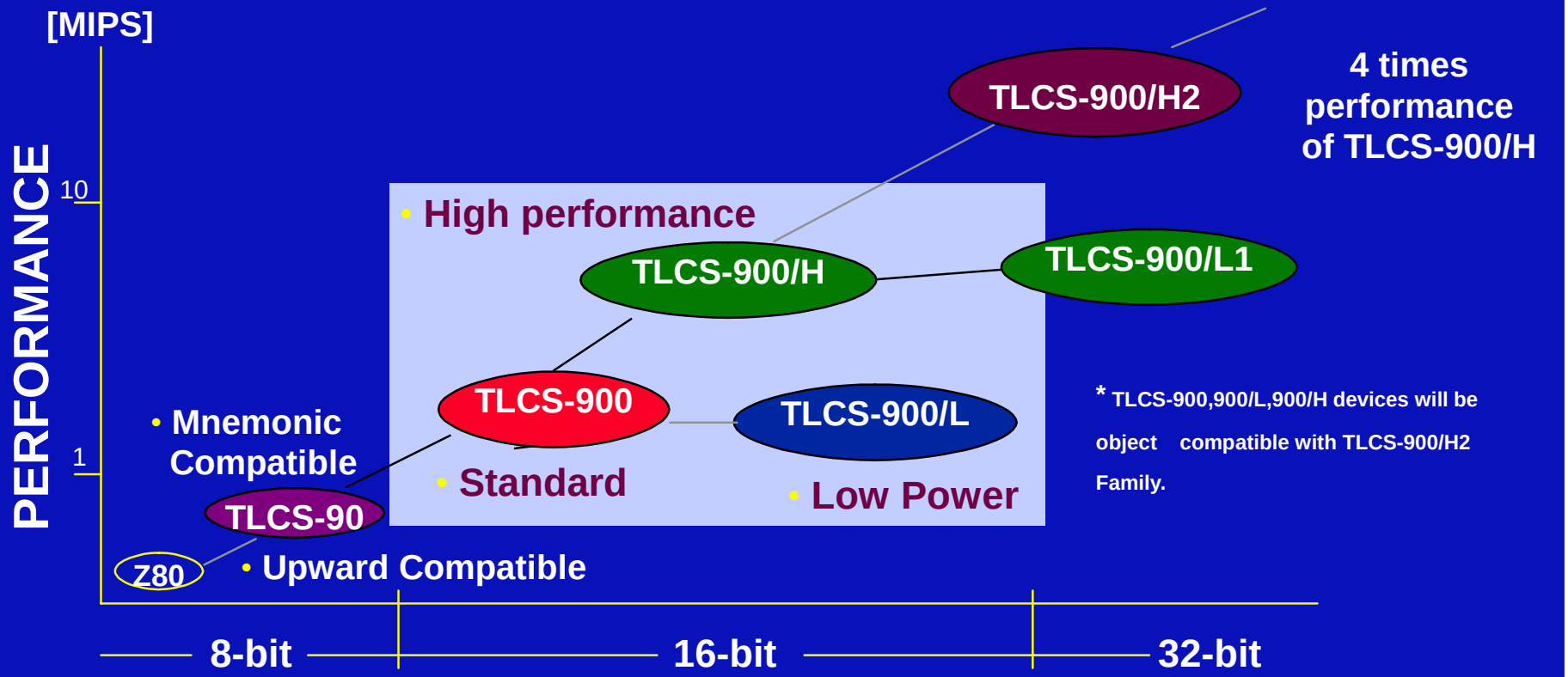
The Family Key Features

- CPU-core : 16/32 Bit
- High-speed processing,
  - ➨ Min. inst. exec. time:
  - ➨200ns (@10MHz) - TLCS-900,900/L
  - ➨160ns (@12.5MHz) - TLCS-900/H,900/L1
  - ➨ 50ns ((@20MHz) - TLCS-900/H2
- Large linear address space *(16M bytes)*
- Powerful instruction set
  - ➨ Regular instruction sets and many addressing modes
- Many bit-processing operations
- Powerful real-time processing
  - ➨ using register banks
- High-speed data transfer using µDMA
- For systems using both 8- and 16-bit buses
  - ➨ dynamic bus sizing function

CPU CORES

TLCS-900

The Road Map



* TLCS-900,900/L,900/H devices will be object compatible with TLCS-900/H2 Family.

TOSHIBA

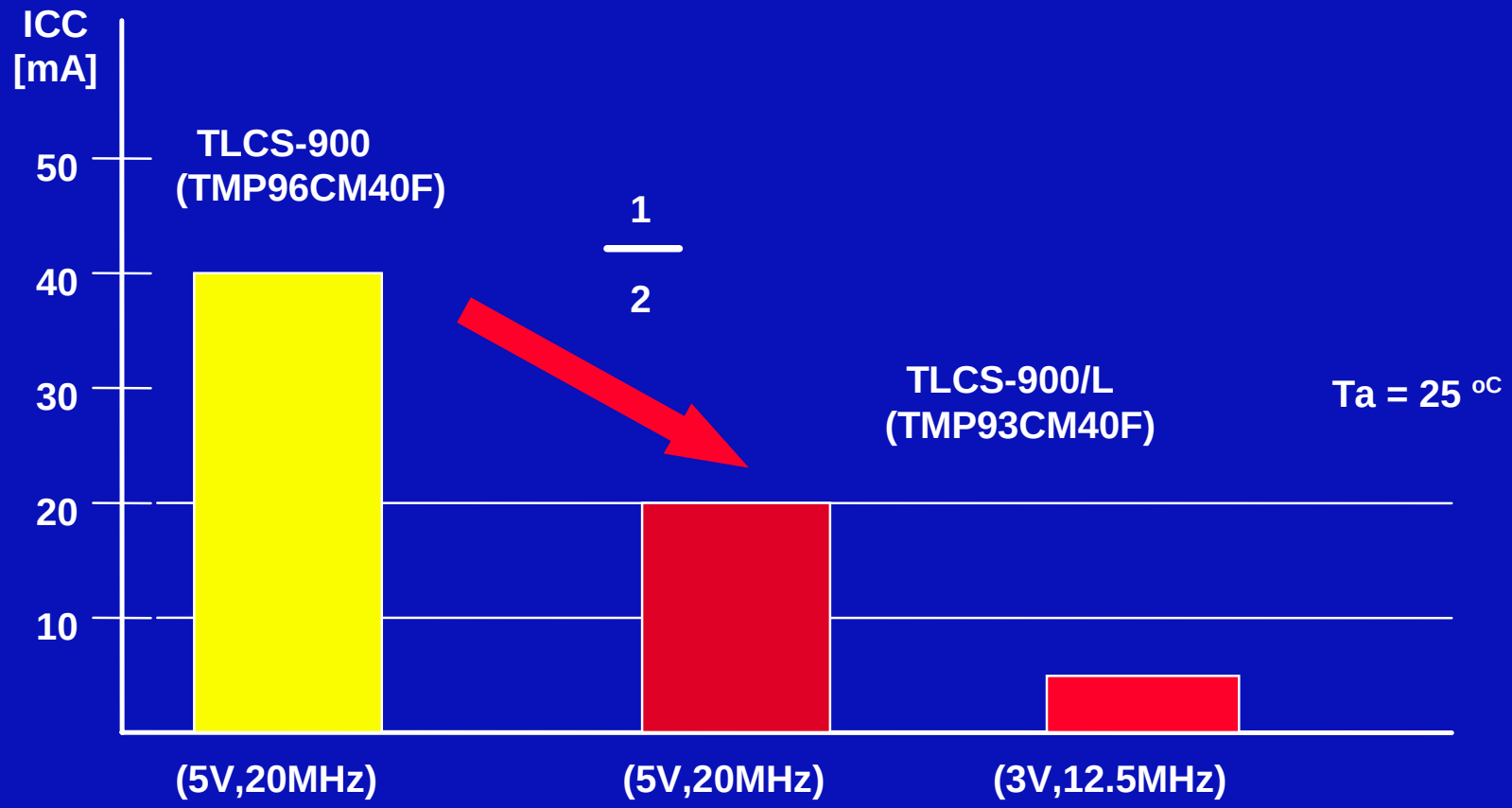
The Family Key Features

ITEM	H2	H & L1	Stand.& L
Max. operating frequency (external)	20 MHz (@10 MHz)	12.5 MHz (@25 MHz)	10 MHz (@20 MHz)
Min. instruction cycle time	50 nsec	160 nsec	200 nsec
uDMA Speed	0,25 usec	0,64 usec	1,6 usec
MULA instruction	0.6 usec	1.52 usec	3.1 usec
Dynamic Bus Sizing	8/16/32 Bit	8/16 Bit	

LOW VOLTAGE OPERATION

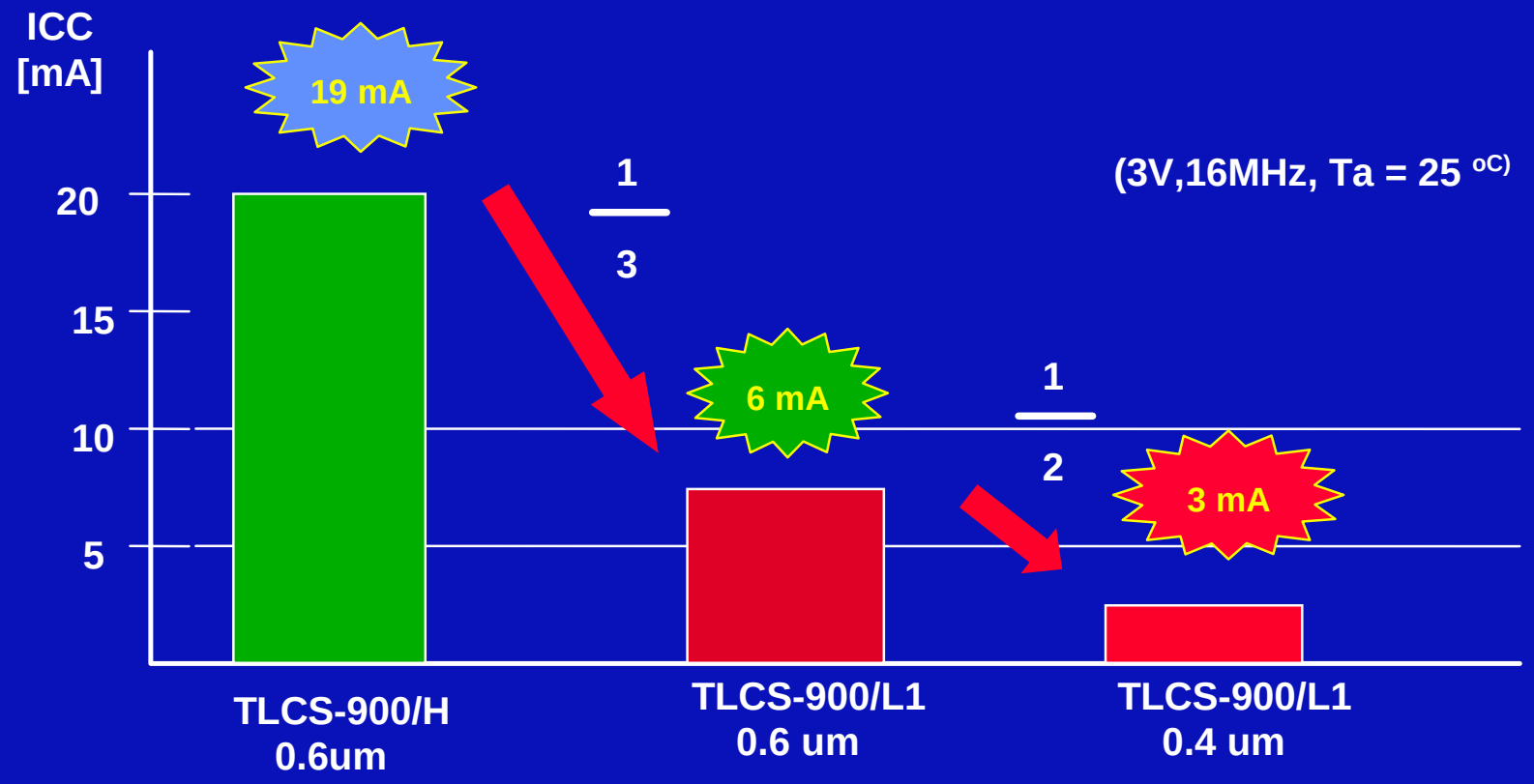
TLCS-900

TLCS-900/L
Low power consumption



TLCS-900

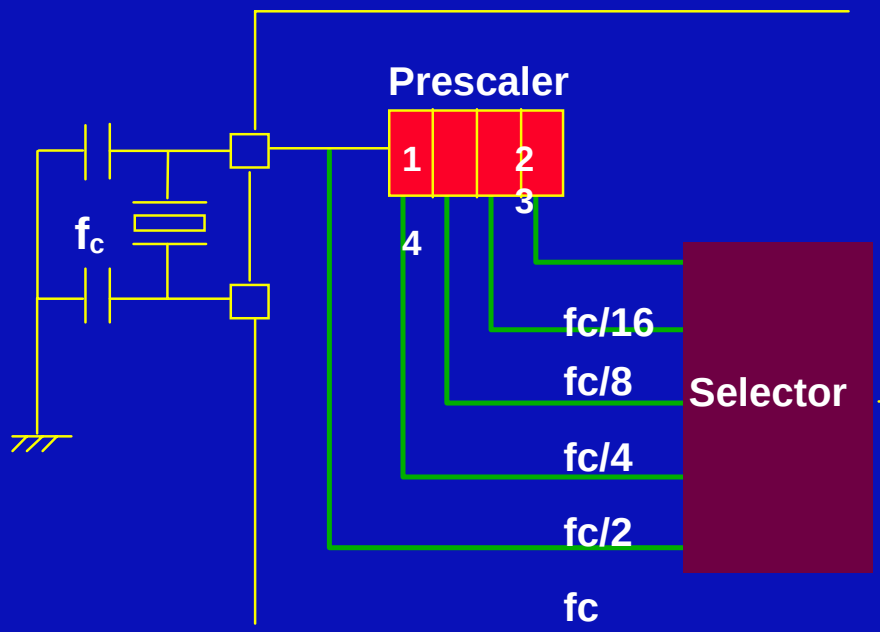
TLCS-900/L1
Low power consumption

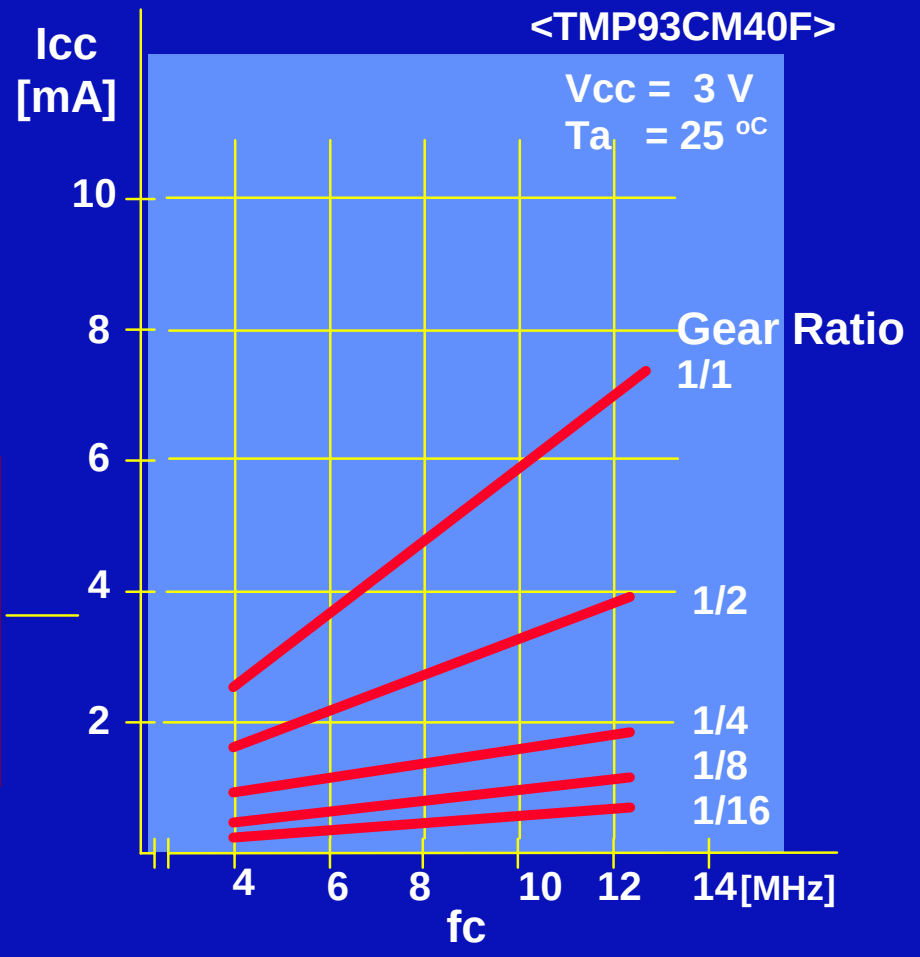


TOSHIBA

TLCS-900

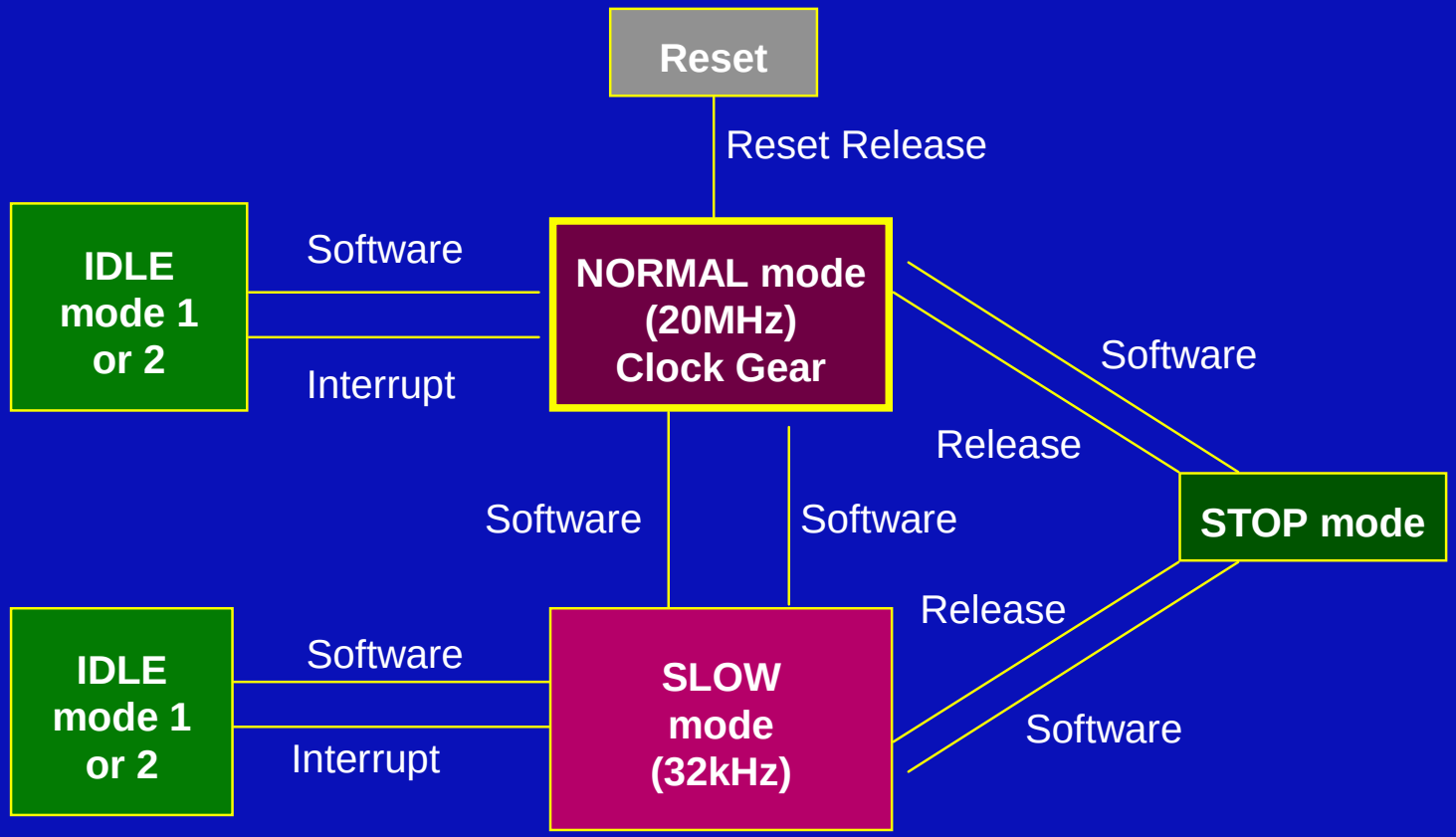
Gear Power Consumption per Software





TOSHIBA

TLCS-900/L : DUAL CLOCK SYSTEM

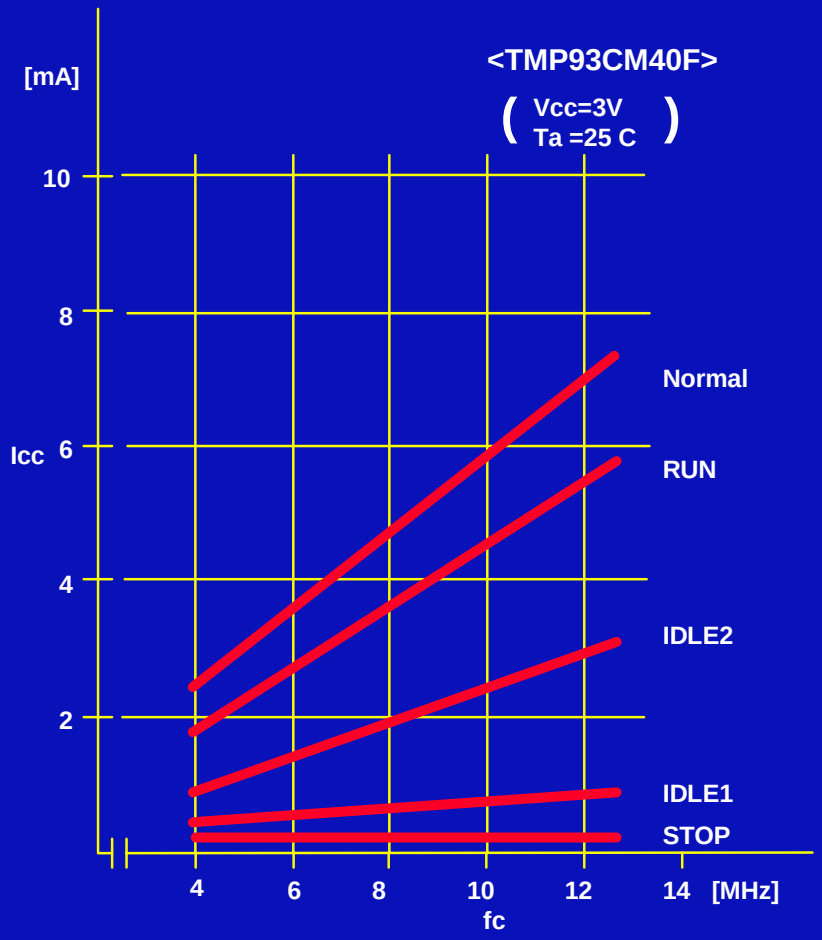


The operation modes

• TLCS-900/L :
4 types of Stand-by mode

Operation mode	CPU	A/D C	Peripheral I/O (Timer,SIO)	Oscillator
NORMAL		O	O	O
RUN		X	O	O
IDLE2		X	X	O
IDLE1		X	X	X	O
STOP		X	X	X	X

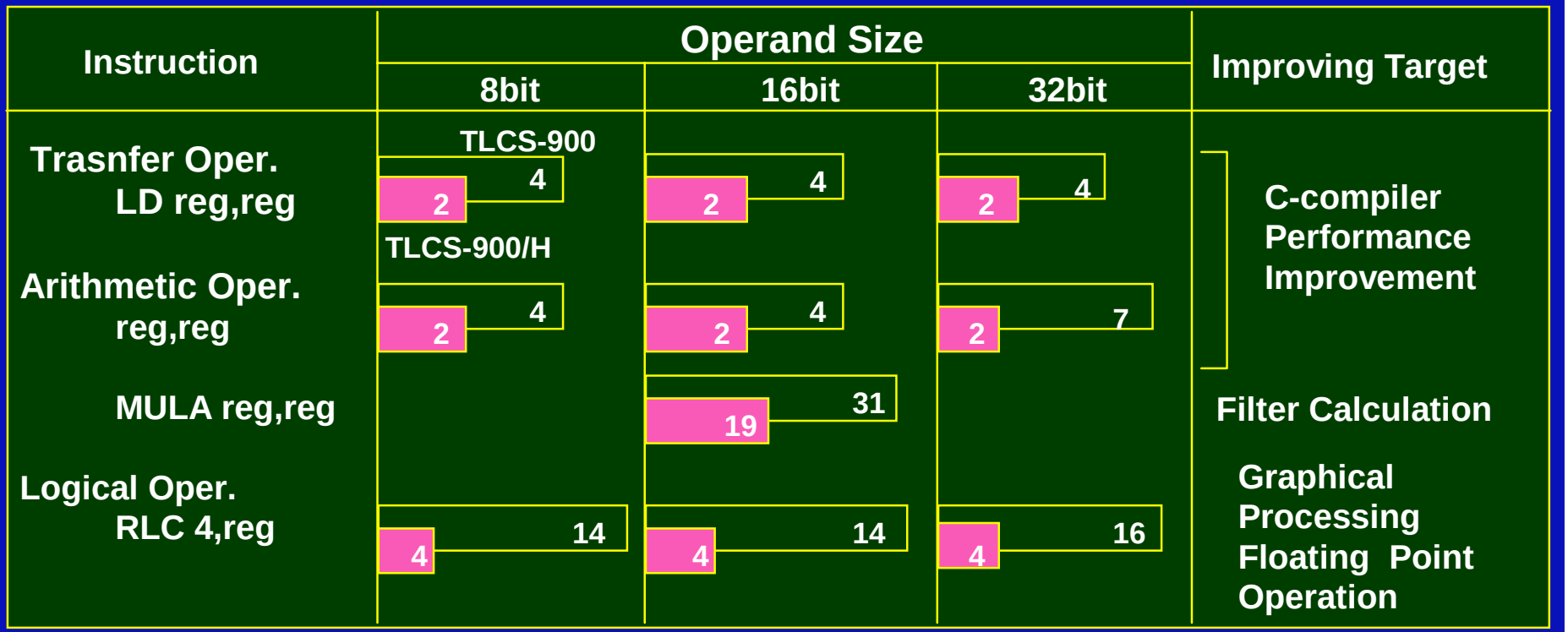
o = operate
x = stop



HIGH SPEED OPERATION

TLCS-900/H
Performance 2 x TLCS-900

Method
- Dual bus
- 32 bit ALU
- 4bit barrel Shifter



< Comparison table of states >

THE 32 BIT TLCS-900/H2 CSIC like RISC

Core comparison “H” V “H2”

CSIC like RISC

High Performance with RISC Technology

	900/H2	900/H
Minimum Execution Instruction Time	50ns	160ns
Internal Clock Frequency	20MHz	12.5MHz
Clock Per Instruction	1 CPI	2 CPI
Internal Data bus	32	16
External Data bus	32	16
Performance Ratio	4	1

CPU - CORE Architecture

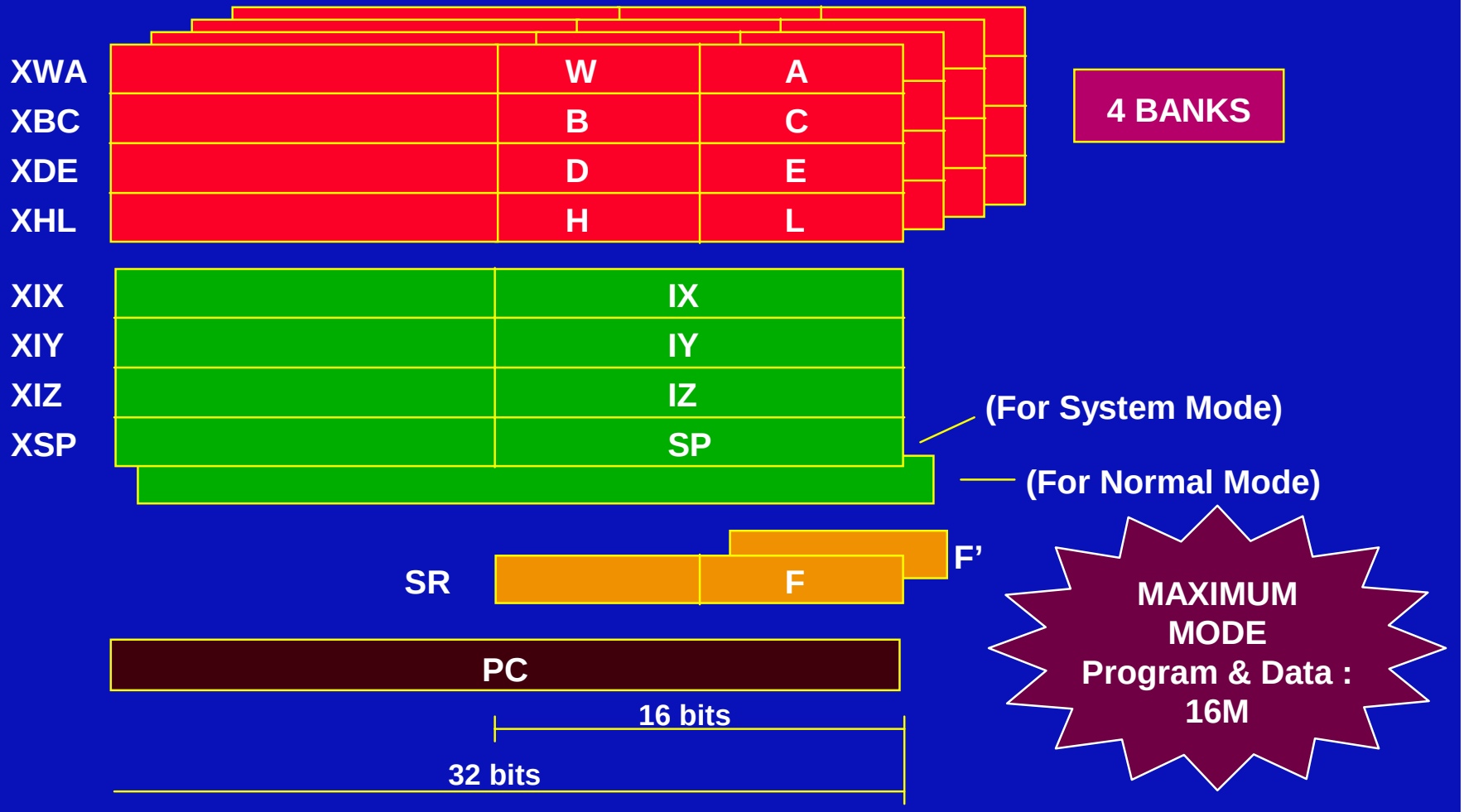
The register configuration (1)

Maximum Mode

- Optimum for systems with program capacity above 64K bytes
  - ➡ Program counter: 32 bits (lower 24 bits are output as address bus)
- Large capacity data space
  - ➡ 16Mbyte addressing can be specified by any general-purpose register
- 32-bit transfer / arithmetic can be executed by general-purpose register
- High Speed image processing/address calculation,etc

TLCS-900

The register configuration (1)

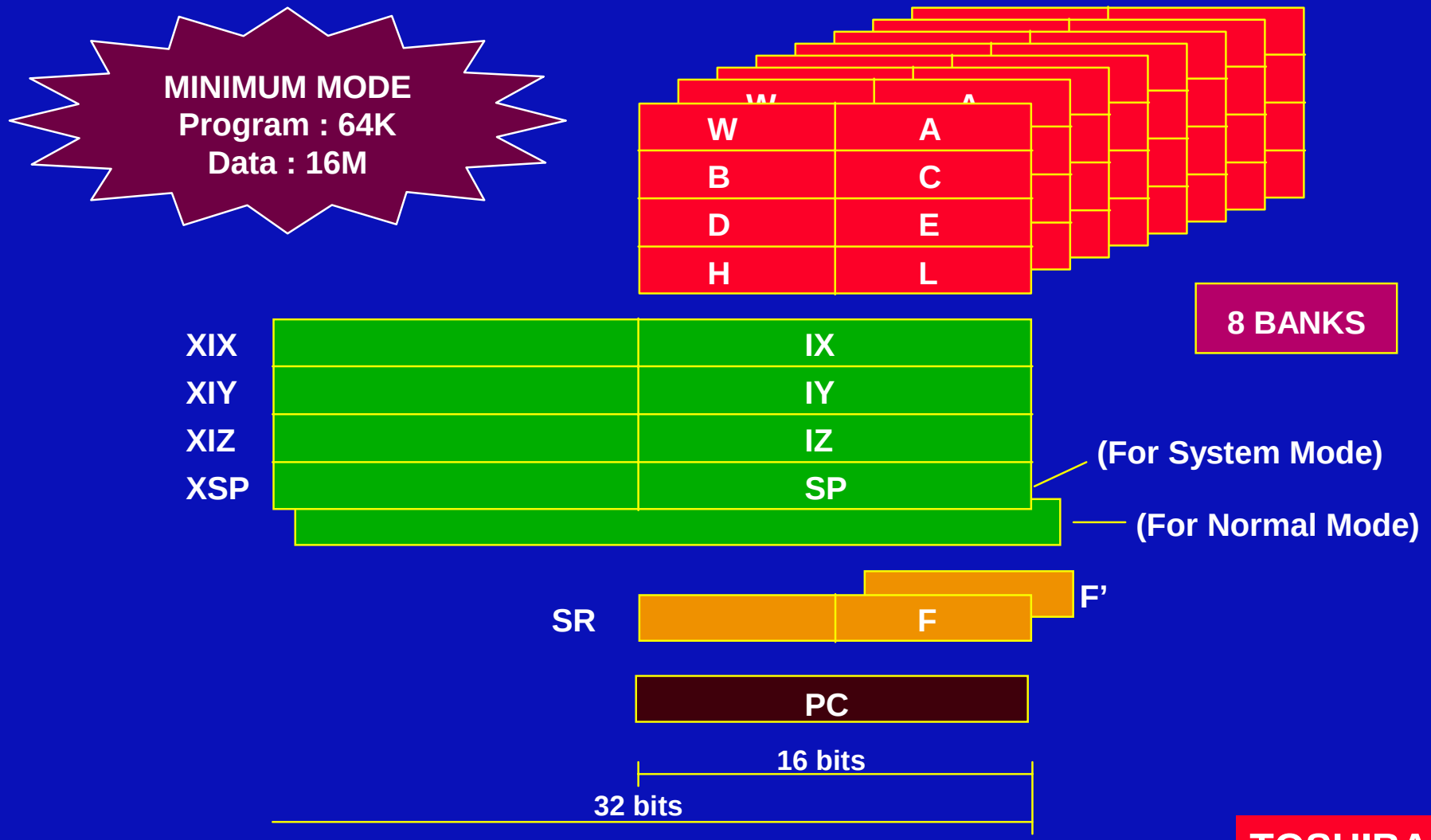


The register configuration (2)

Minimum Mode

- Optimum for systems with program capacity less than 64K bytes
  - Program counter: 16 bits
- Large number of bank registers
  - 16 bits x 4 registers x 8 banks
- Large data capacity
  - Expandable up to 16M bytes
  - Accessible to data area above 64K bytes using XIX, XIY, XIZ, XSP registers
- Capable of addressing with WA, BC, DE, HL, registers.

The register configuration (2)



Instruction set examples

- Filter operation instruction
  - MULA: 16 Bits x 16 Bits/32 Bits-32Bits (3.1us @ 20MHz) (signed multiplication-addition arithmetic)
  - MINC: Modulo increment...For circulating buffer pointer increment (Increments lower n bit only. 1 <= n <= 16)
  - MDEC: Modulo decrement...For circulating buffer pointer decrement (Decrements lower n bit only. 1 <= n <= 16)
- Logical operation instructions
  - AND/OR/XOR: And/or/exclusive-or of 8, 16, and 32 bits

Instruction set examples

continued.....

- Bit operation instructions

– BIT/SET/RES/CHG: Bit test/set/reset/invert

– LDCF/STCF: Transfer between carry flag and any given bit

– ANDCF: And of carry flag and any given bit

– ORCF: Or of carry flag and any given bit

– XORCF: Exclusive-or of carry flag and any given bit

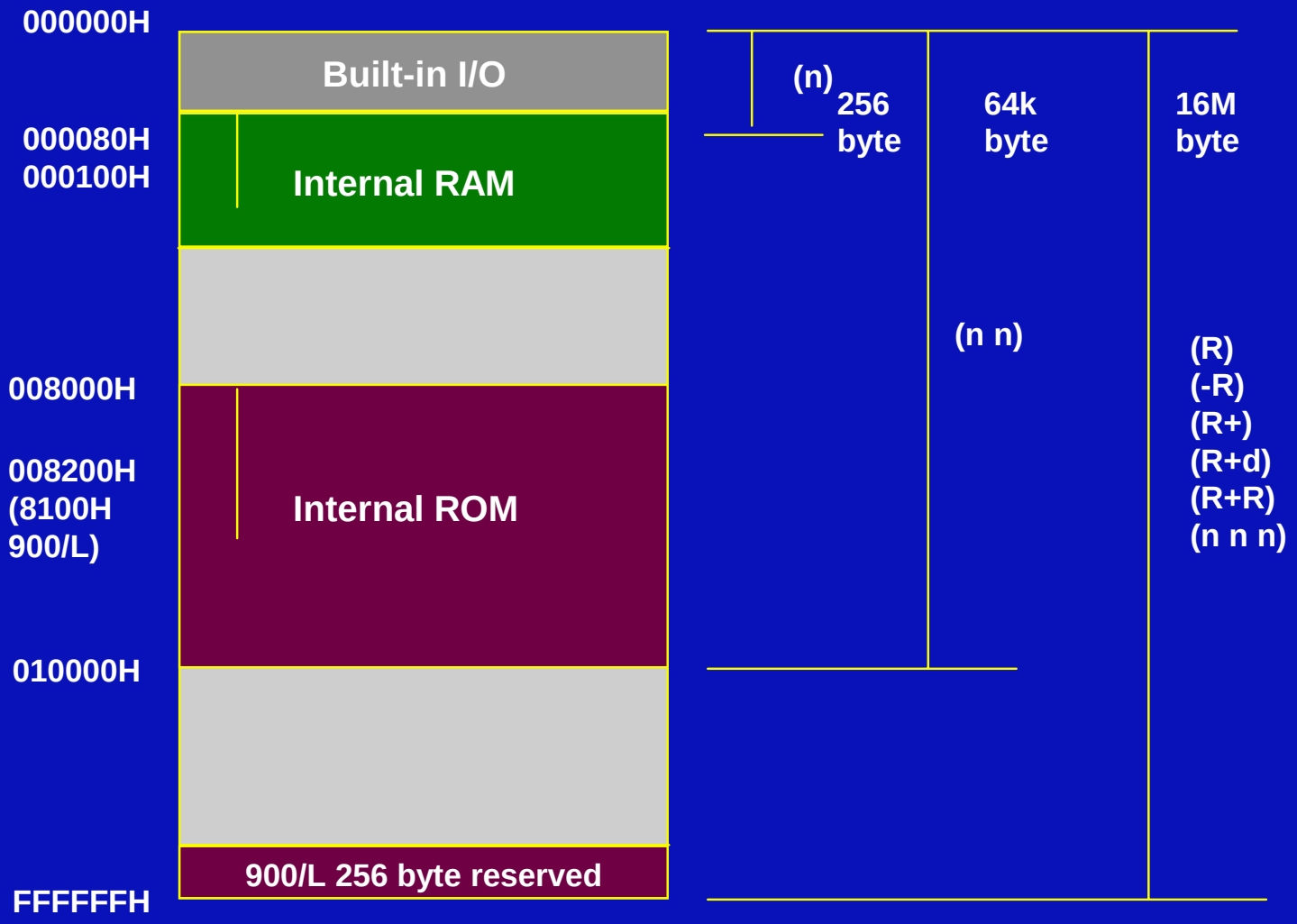
– BS1: Searches bit pattern for 1.

High -Speed Processing

Family	900 & 900/L 10 MHz	900/H & 900/L1 12.5 MHz	900/H2 20 MHz	Function
Instruction				
LD r, #8	200ns	160 ns	50 ns	8-bit transfer
LD XHL, xrr	400ns	160 ns	50 ns	32-bit transfer
AND XHL, (mem)	400ns	320 ns	100 ns	16-bit operation
ADD HL, rr	700ns	160 ns	50 ns	32-bit operation
SET b, (mem)	800ns	560 ns	200 ns	bit set
MUL HL, #16	2.6µs	1.2 µs	450 ns	16 bits * 16 bits
DIV XHL, #8	3.0µs	1.84 µs	650 ns	32 bits / 16 bits
MULA rr	3.1µs	1.52 µs	600 ns	16*16 +32 bits
CALL #24	1.2 µs	800 ns	200 ns	Direct Call
JP #24	700 ns	480 ns	100 ns	Direct Jump

TLCS-900

The memory map



The Interrupt (1)

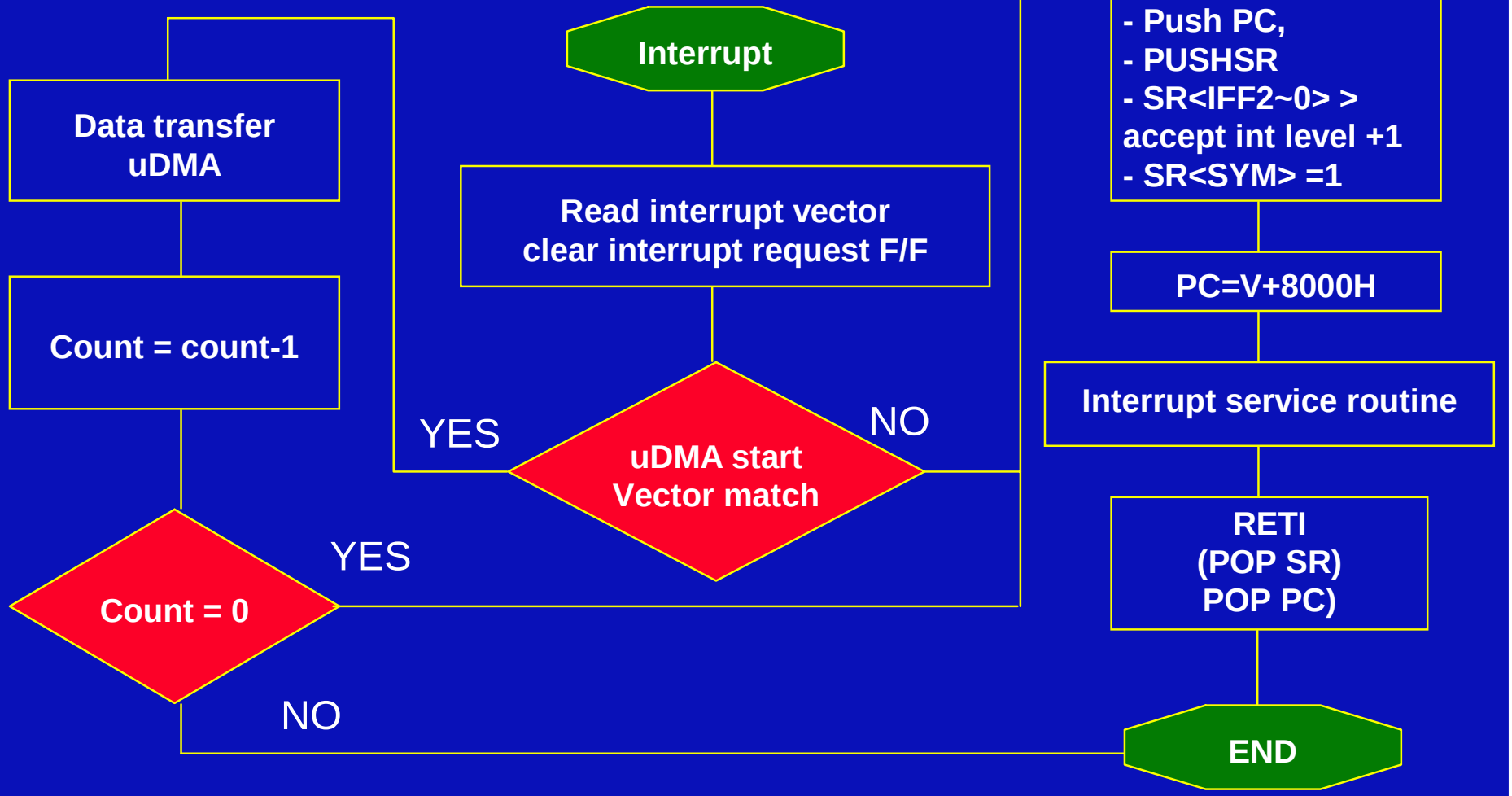
- Priority level (0 to 7) can be set for each interrupt source.
- Non-maskable interrupts
  - Software interrupts (SWI0 to 7)
  - NMI pins
  - Watchdog timer
  - Privileged or undefined instruction violation
- Maskable interrupts
  - External pins (INT 0,1,2,..)
  - Internal I/Os: DMA
  - Timer
  - SIO
  - A/D converter

High-speed µDMA

- DMA implemented using CPU block executed directly from microcode
- Speed equivalent to DMA controller
  - 1- 2- byte transfer:
    - 1.6us (@20MHz) TLCS-900,900/L
    - 640ns (@25MHz) TLCS-900/H
- Supports 4-channels, 16Mbyte address space
- Maximum number of transfer blocks: 64k words

- Many transfer modes:
  - 1) I/O to memory : (R-
bytes
  - 2) I/O to memory : (R-
bytes
  - 3) memory to I/O : (R)
bytes
  - 4) memory to I/O : (R)
bytes
  - 5) I/O to I/O :
bytes

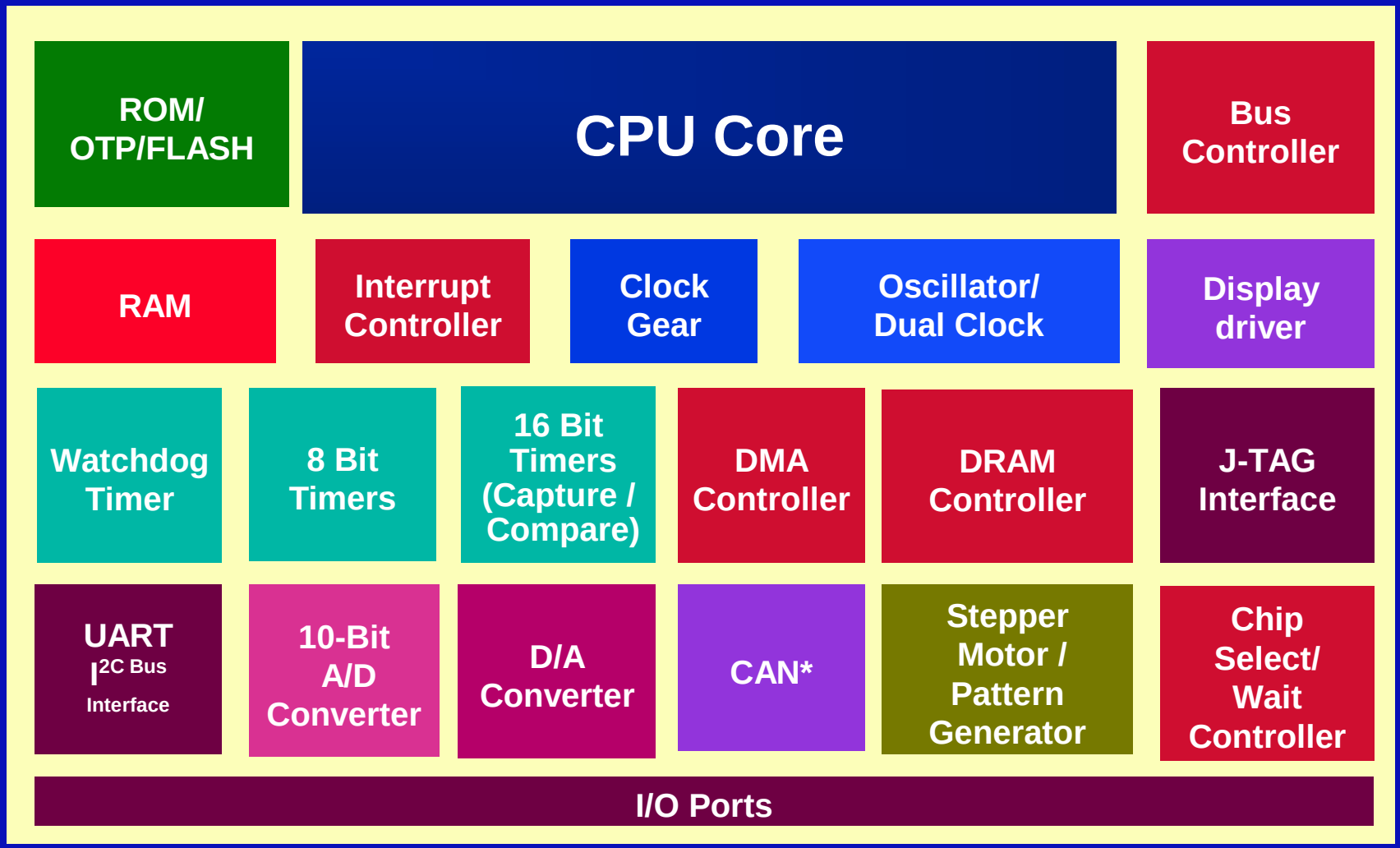
The Interrupt (2)



PERIPHERALS

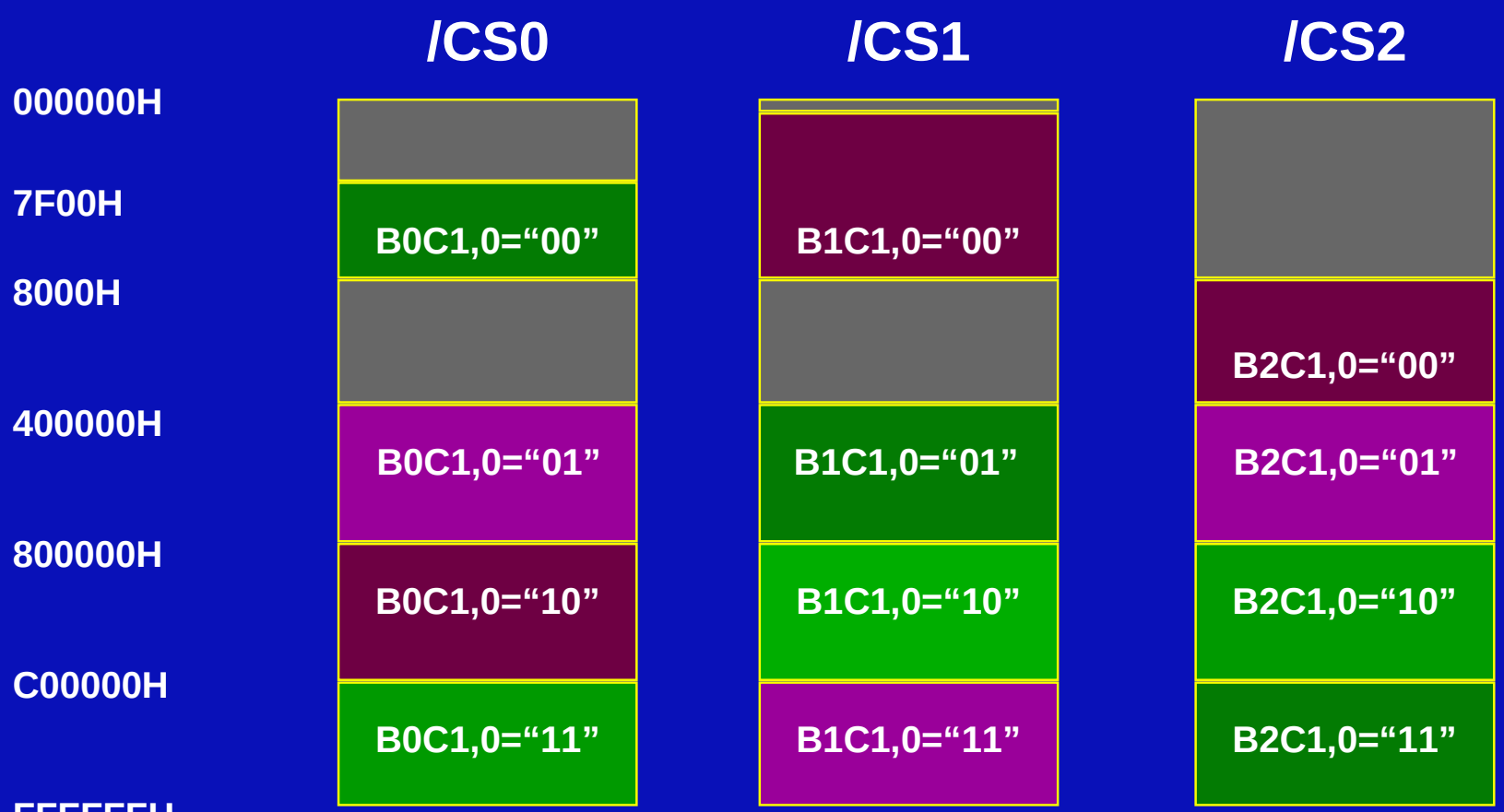
TLCS-900

The Peripherals



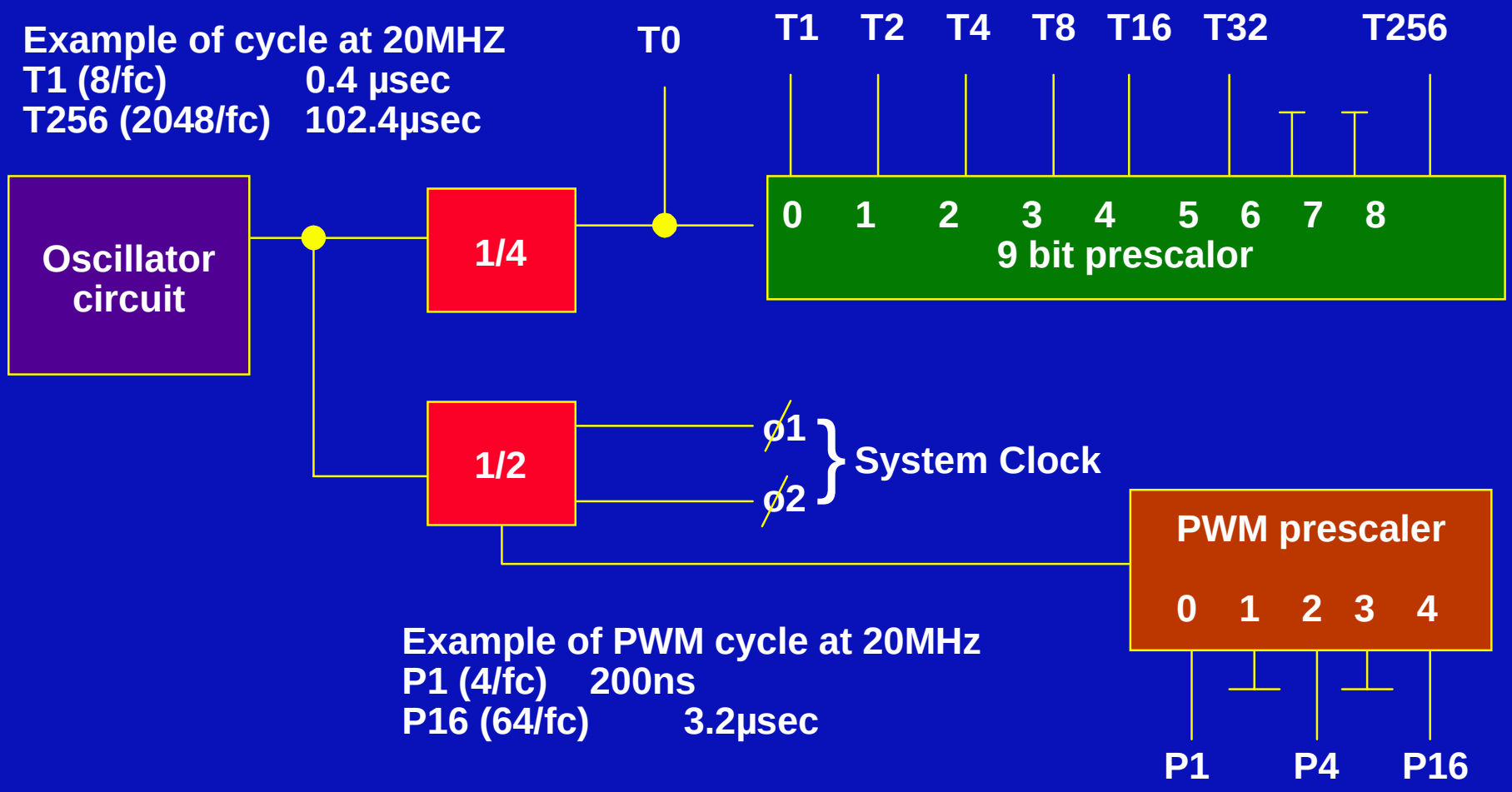
* Under Development

The chip select image



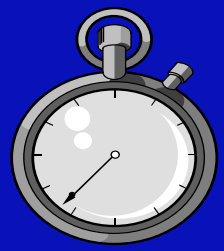
TLCS-900

The Prescaler



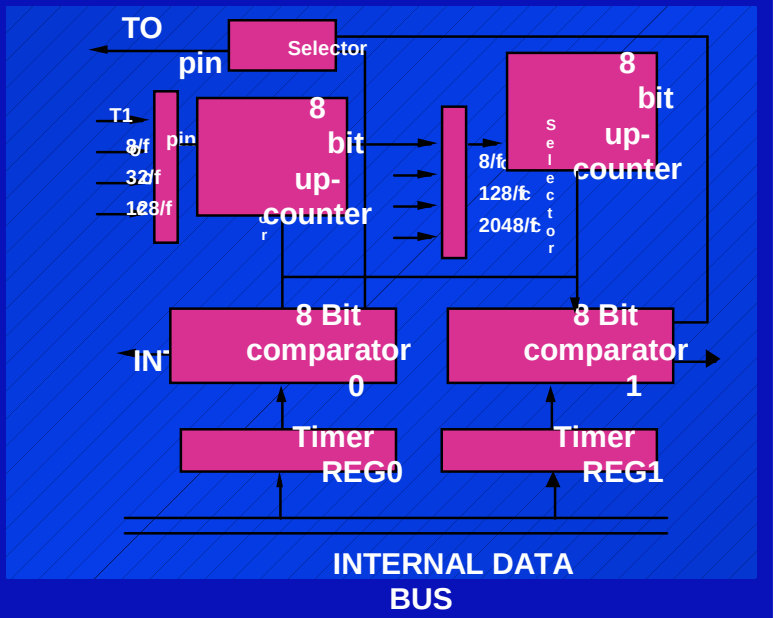
TOSHIBA

8 Bit Timer

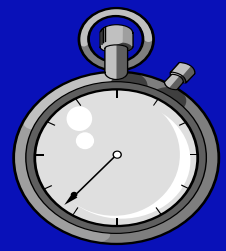


By cascading two 8-bit timers, a 16-bit timer can be configured.

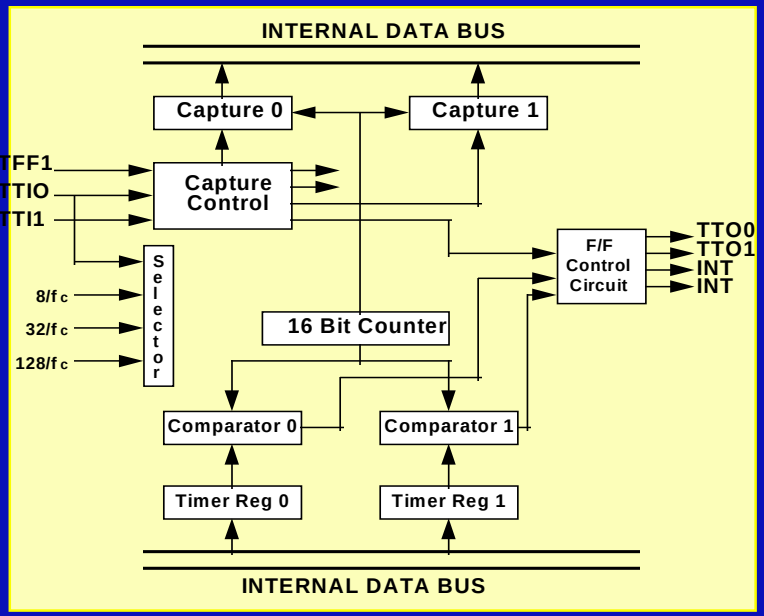
- 8-bit interval timer mode (x2)
- 16-bit interval timer mode (x1)
- 8-bit programmable square wave
  - (PPG: variable duty with variable cycle) output mode (x1)
- 8-bit PWM
  - (Pulse width Modulation):Variable duty with constant cycle) output mode (x1)



16 Bit Timers /event counters



- 16 bit interval timer mode
- 16-bit event counter mode
- 16-bit programmable square wave output (PPG) mode
- Frequency measurement mode
- Pulse width measurement mode
- Time difference measurement mode

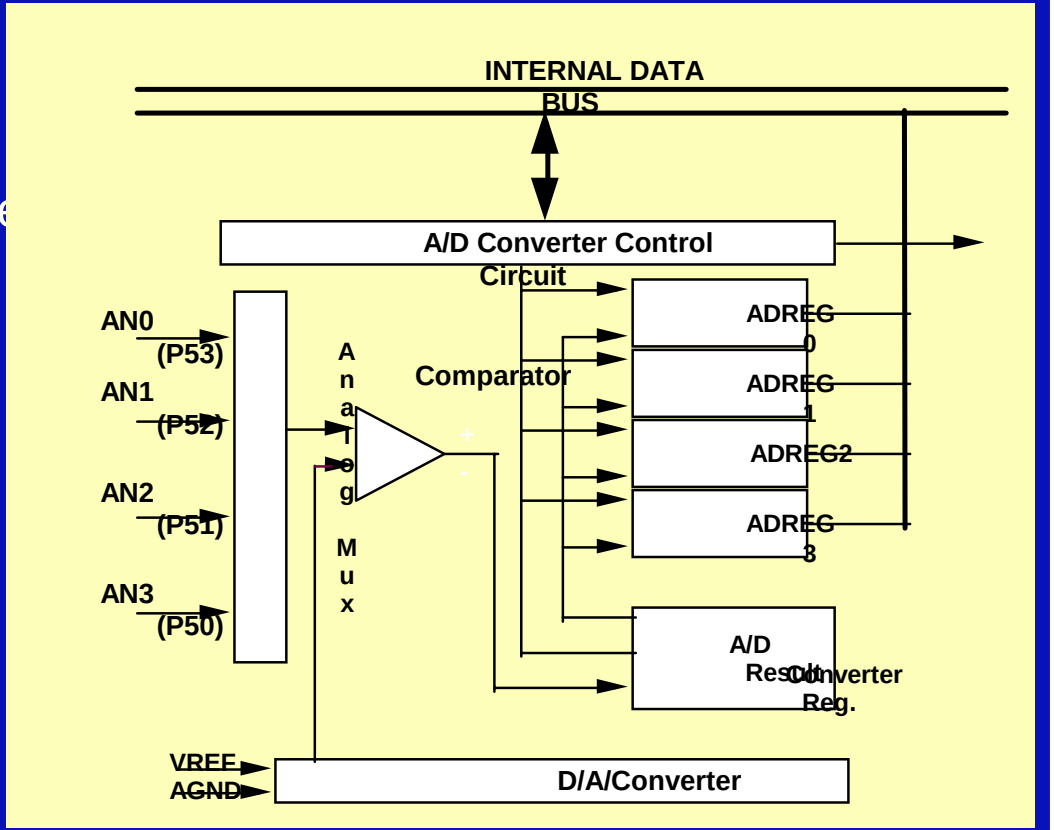


- A timer event counter consists of the following:
  - 16-bit up counter
  - two 16-bit timer registers
  - two 16-bit capture registers
  - two comparators
  - capture input control
  - timer F/F and its control circuit

TOSHIBA

A/D Converter

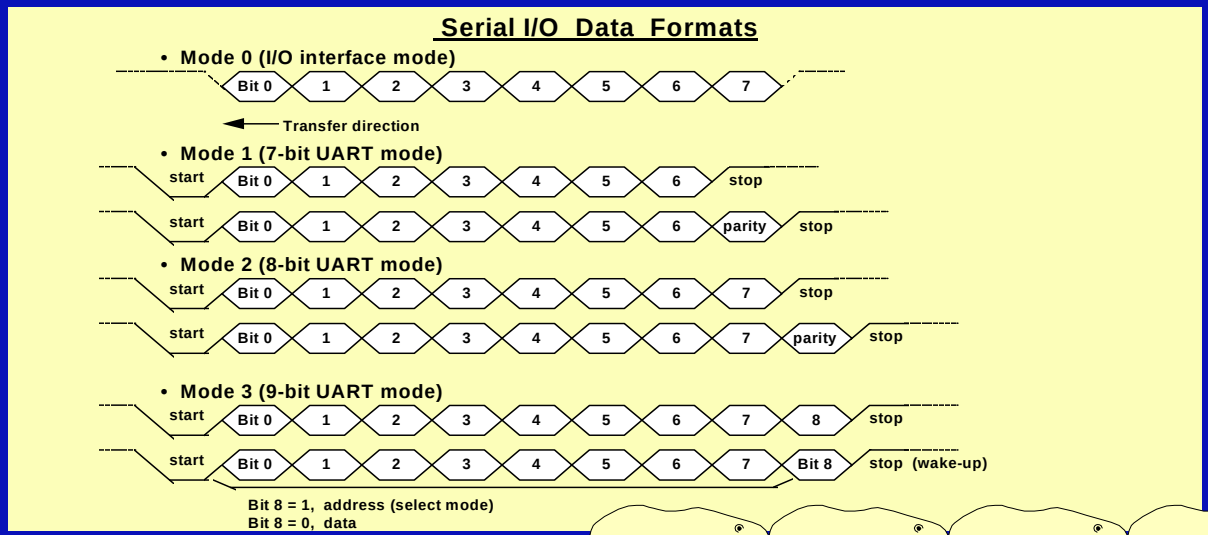
- 4 to 16 channel 8 or 10 bit resolution (by Product)
- Successive approximation syste
- High speed conversion
  - 16µs to 3 µs (by product)
- 4 conversion modes
  - Single channel mode
  - Channel scan mode
  - Single mode
  - Repeat mode
  - Flag/Interrupt operation

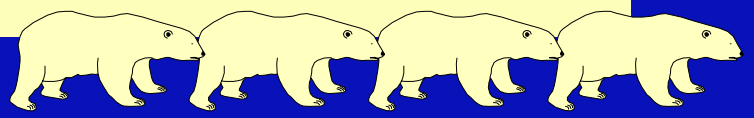


TOSHIBA

Serial I/O

- UART mode (x2): 7/8 & 9 bit modes, internal BRG/timer O clock
  - Max. baud rate: 500 kbps@ 16MHz using o1
- Synchronous (I/O interface) mode: 8 bits internal/external clock
  - Max clock: 1.25Mbps
- I2C-Bus Interface

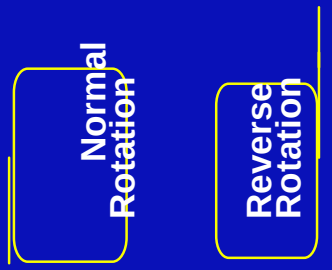


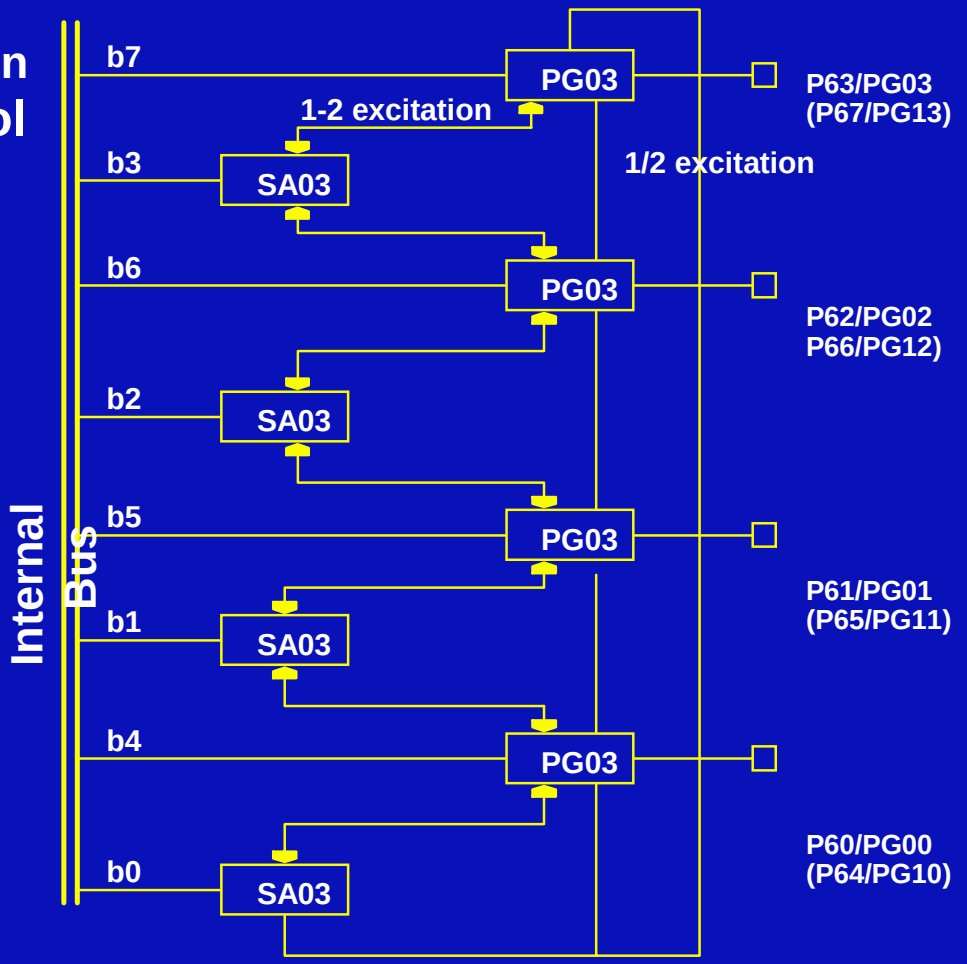


TOSHIBA

The pattern generator

- 2 channels, 4bits/channel
- General purpose pattern generation
- Hardware stepper motor control (eg. 4-phase 1-step/2-step excitation)



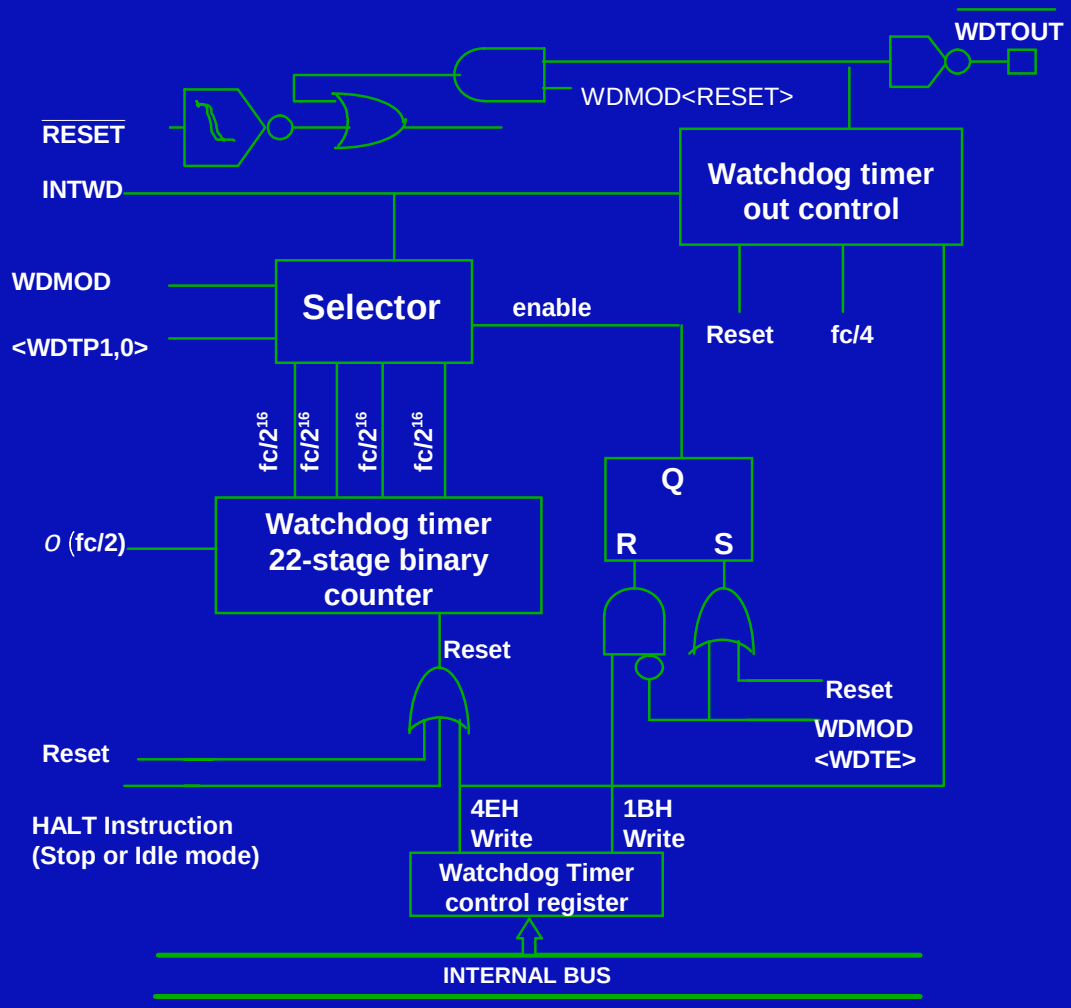


Difference between PG0 & PG1

	PG0	PG1
Trigger Signal	From Timer 4	From Timer 5

The Watch dog timer

- Generates NMI to CPU
- WDTOUT signal for application
- 22 - stage binary counter choice of 4 outputs
  - (2^{16} /fc, 218 /fc 220 /fc, 222 /fc)



examples:

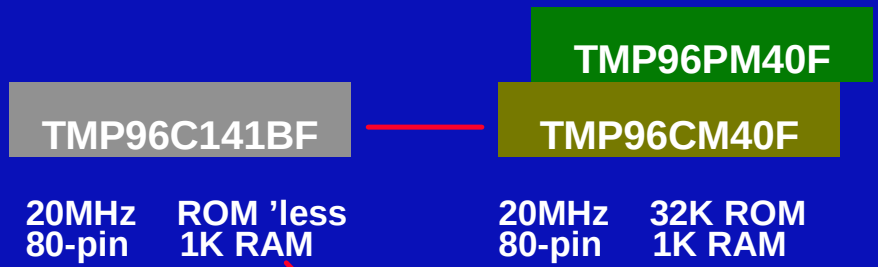
2^{16} /fc = 32,768 states (approx. 3.3ms @ 20MHz);

222 /fc = 2M states (approx. 210ms @ 20MHz)

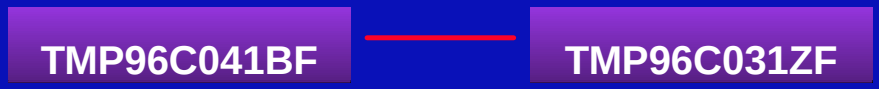
THE ROAD MAP

TLCS-900

Standard family line up



MNEMONIC
COMPATIBLE



TLCS-90

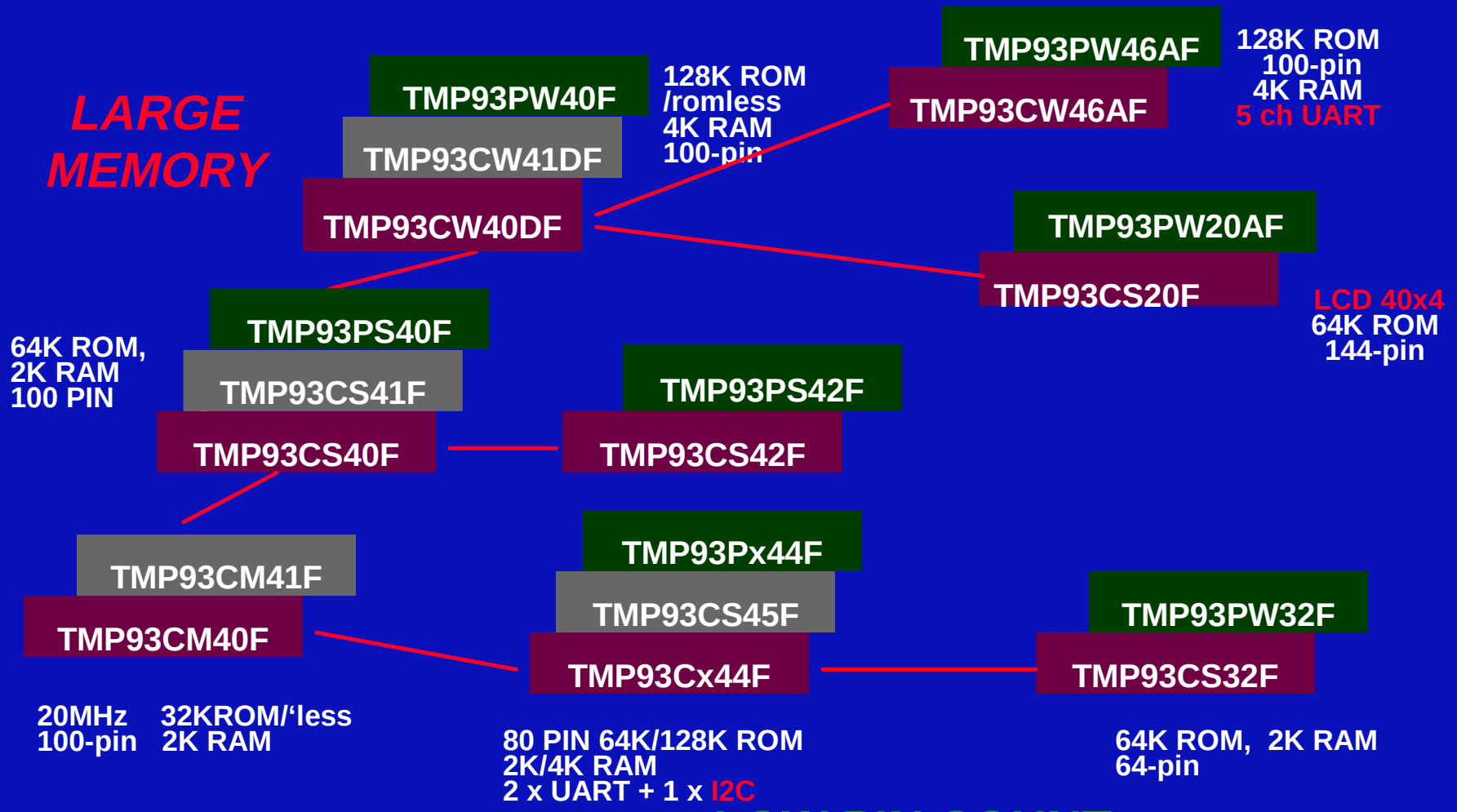
8-Bit MCU

Small package

TOSHIBA

TLCS-900

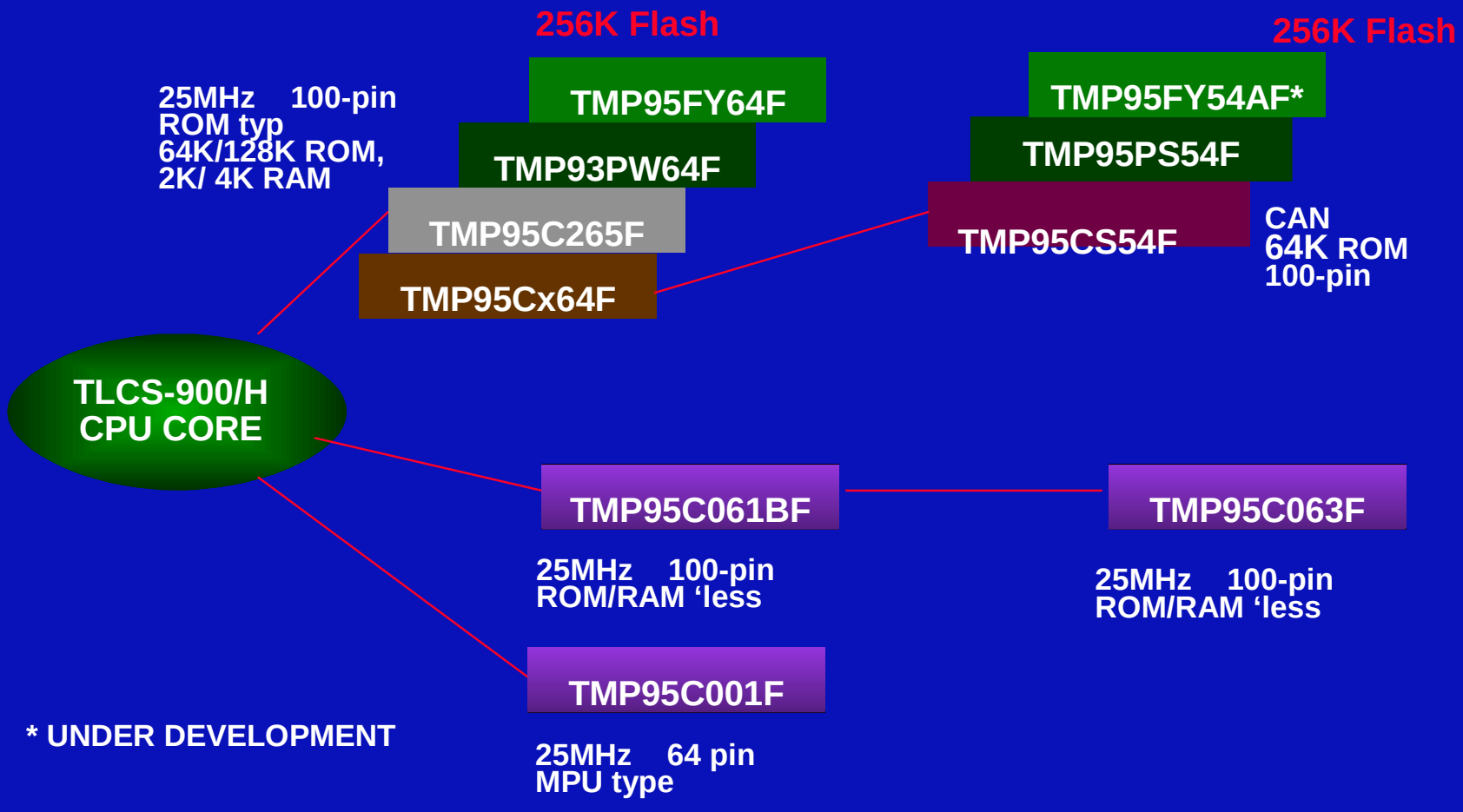
TLCS-900/L- DEVELOPMENT TREND



TOSHIBA

TLCS-900

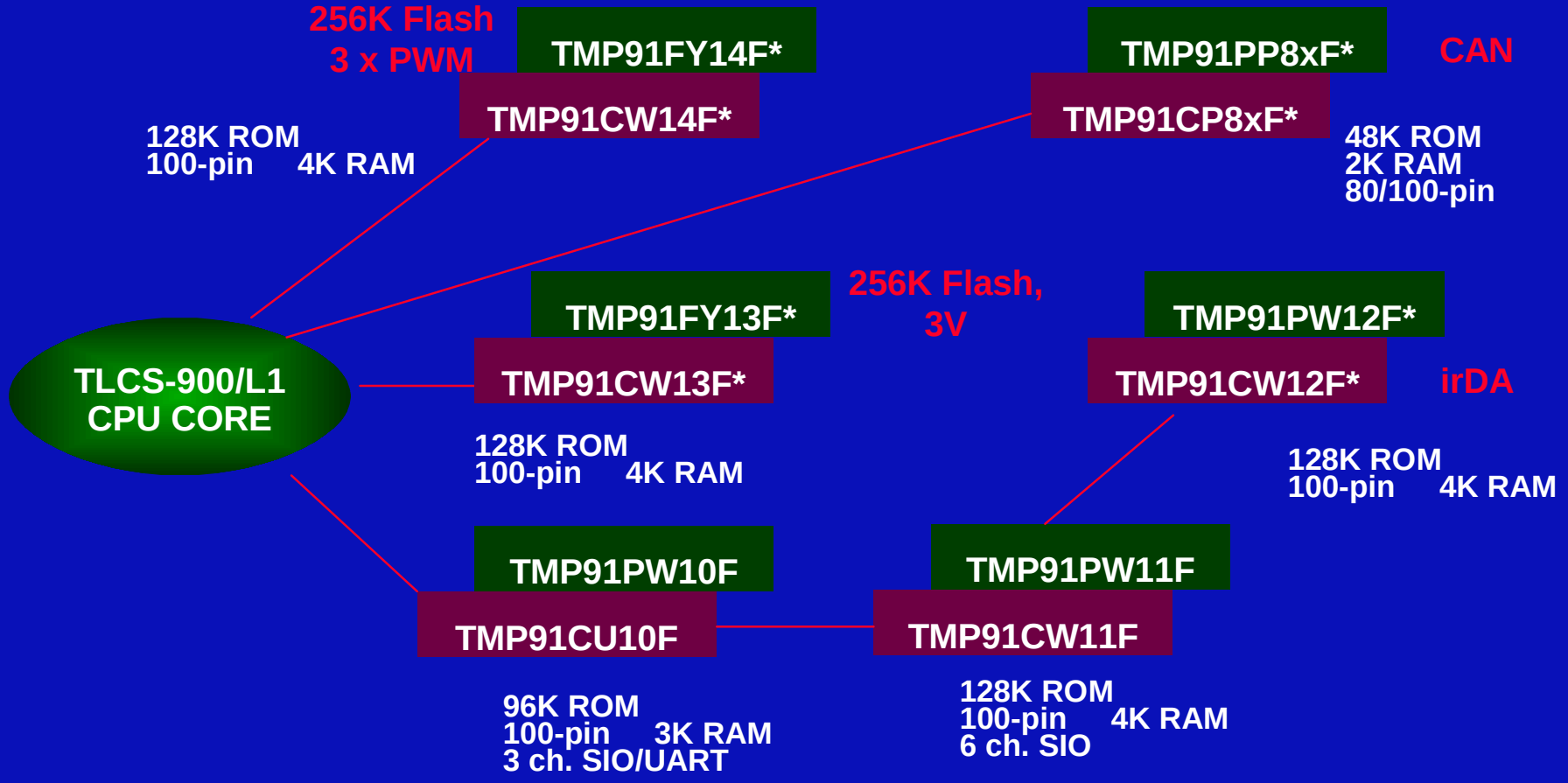
TLCS-900/H Development trend



TOSHIBA

TLCS-900

TLCS-900/L1 Development trend

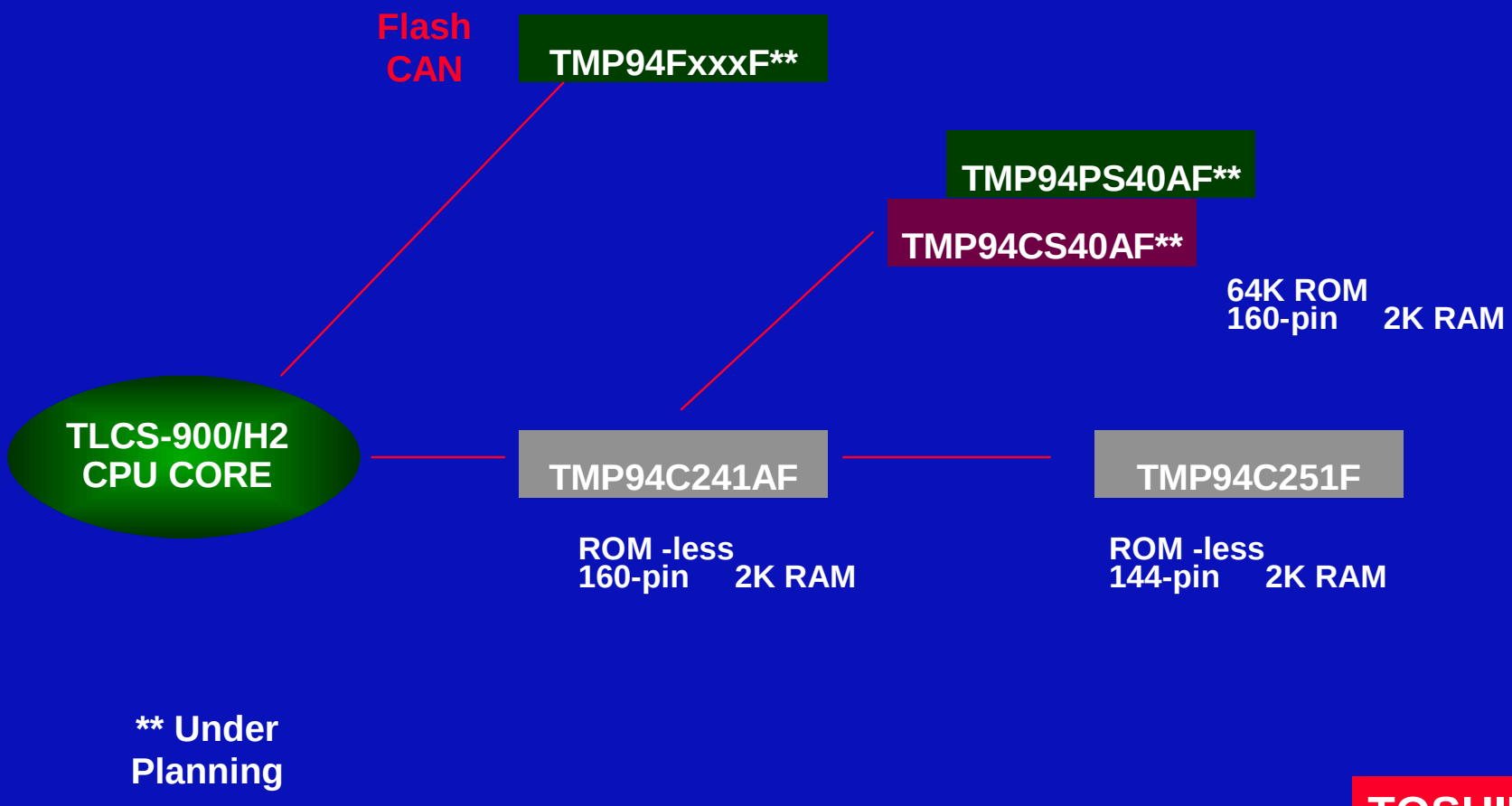


* UNDER DEVELOPMENT

TOSHIBA

TLCS-900

TLCS-900/H2 Development trend



** Under Planning

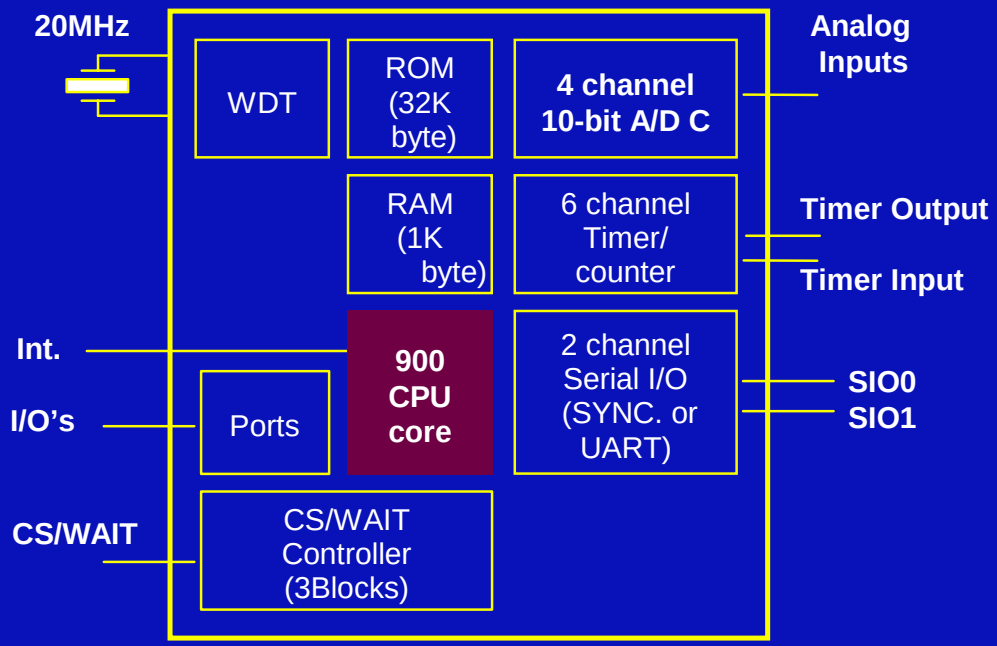
TOSHIBA

THE PRODUCTS

TLCS-900

TMP96C141 group

- TLCS-900 core
  - Min. Instruction Exec. Time = 200ns (@20MHz)
- Address Space
  - Program : 16M Byte
  - Data : 16M Byte
- µDMA : 1.6µs / 2Byte
- Dynamic Bus Sizing
- Peripherals
  - 16bit Timer x 2ch Capture x4, Compare x4
  - Serial I/O : 2ch. (Clocked I/O or UART)
- Package : QFP80



Memory variation

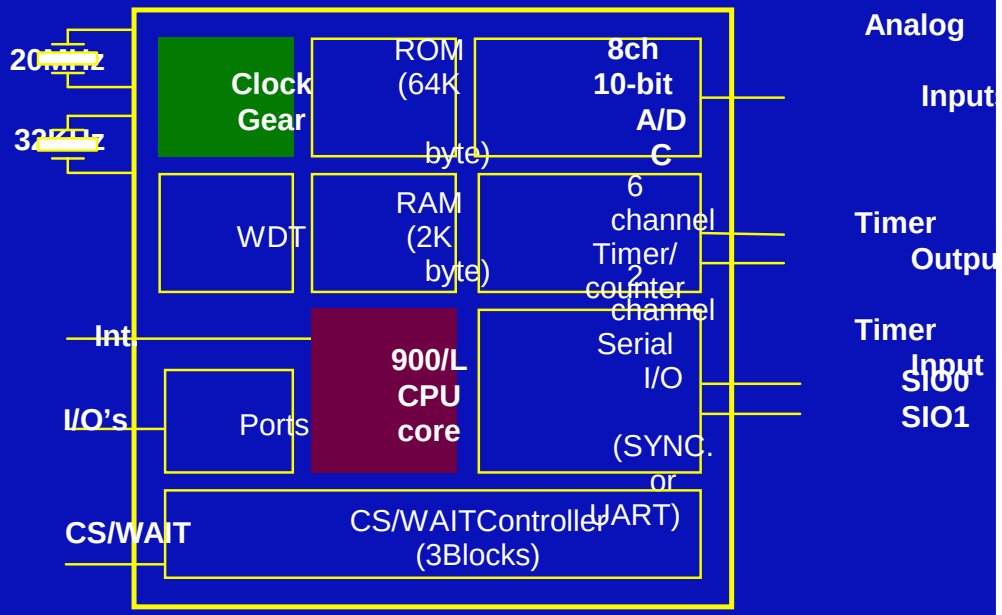
Type	ROM (byte)	RAM (byte)	I/O's	
TMP96C141BF	-	1024	47	
TMP96CM40F	32K	1024	65	
TMP96PM40F	32k(OTP)	1024	65	
TMP96C041BF *	-	-	47	

TOSHIBA

TLCS-900

TMP93Cx40F group

- TLCS-900/L core
  - Min. Instruction Exec. Time 200ns(@20MHz)
- Linear address space
  - Program/Data:16M Byte
- Dynamic Bus Sizing
- Low Power Operation
  - Clock Gear
  - Dual Clock
  - 4 stand-by modes
- 10bit A/D Converter
- 2 UARTS/SIO
- Package :
  - 100 pin LQFP
  - 100 pin VQFP



Memory variation

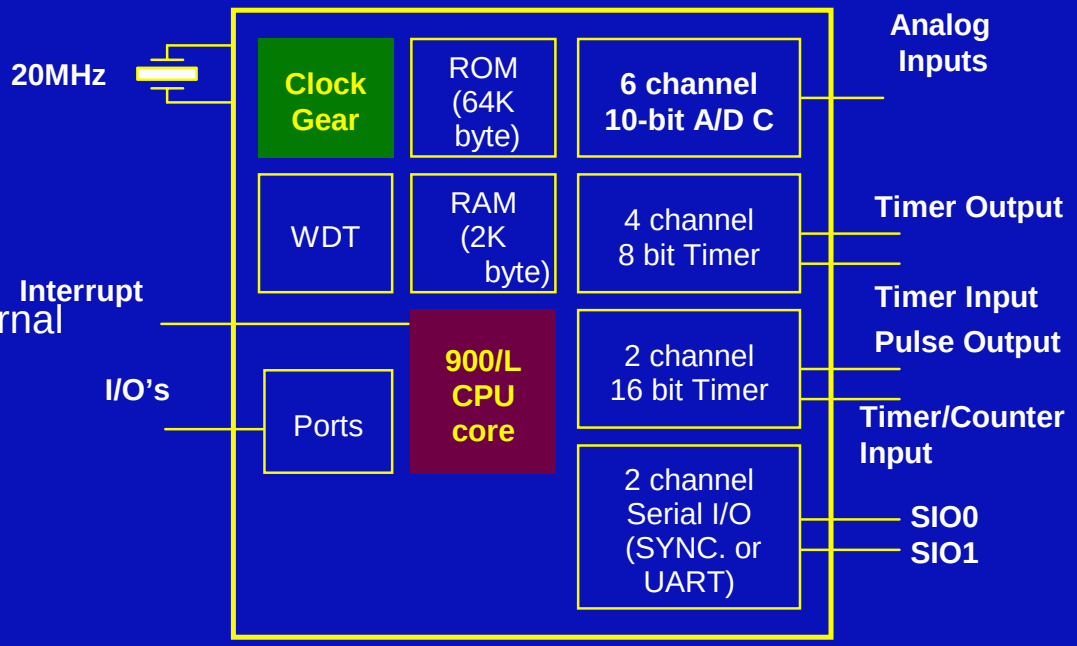
Type	ROM (byte)	RAM (byte)
TMP93CM40F	32k	2048
TMP93CM41F	-	2048
TMP93CS40F/DF		64k
		2048
TMP93PS40F/DF		64k(OTP)
		2048
TMP93CW41F	-	4096
TMP93CW40F		128k
		4096
TMP93PW40F		128k(OTP)
		4096

TOSHIBA

TLCS-900

TMP93Cx32F

- TLCS-900/L core
- Low Power Operation
  - Clock Gear
  - 4 stand-by mode
- 10bit A/D Converter
  - 6. ch, Conv. Time = 8µs, External trigger
- LED drive : 2ch x 10 mA
- Package : 64 pin QFP



Memory variation

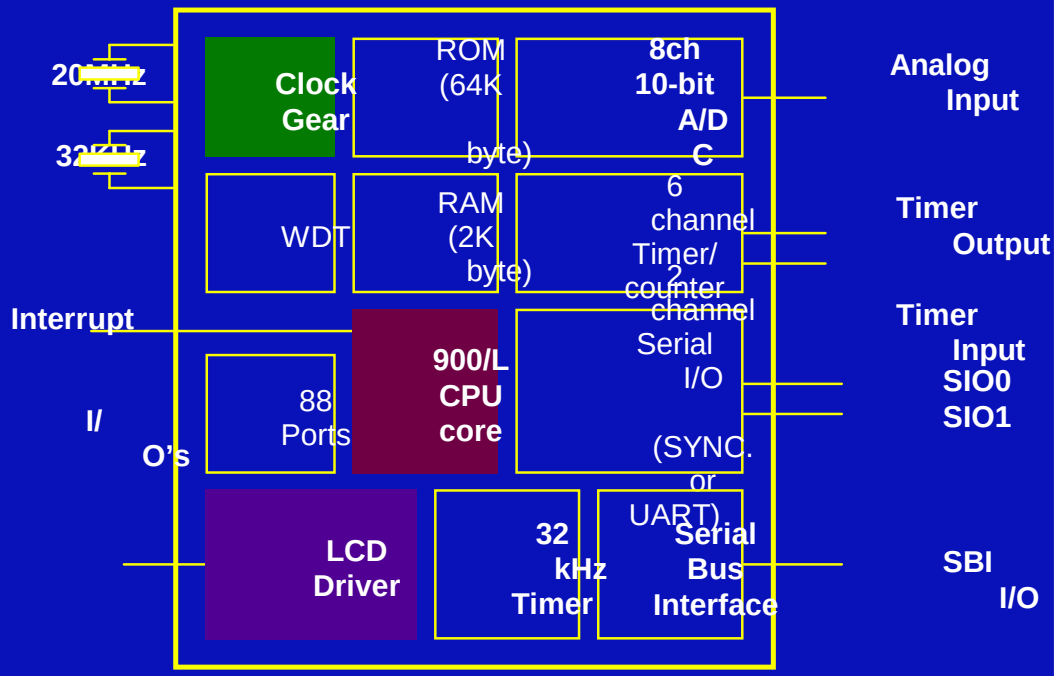
Type	ROM(byte)	RAM(byte)	
TMP93CS32F	64K	2048	
TMP93PW32F	128K(OTP)	4096	

TOSHIBA

TLCS-900

TMP93CS20F

- TLCS-900/L core
- LCD driver
  - 40 seg. X 4 com.
- 10bit A/D Converter
  - Conv. Time = 8 µs
  - External trigger
- 32 kHz Timer
- Low Power Operation
  - Clock-Gear function
  - Dual-clock (20MHz,32kHz)
  - 4 stand-by mods
- Package :
  - 144 QFP (20 x 20 x 1.4t)



Memory variation

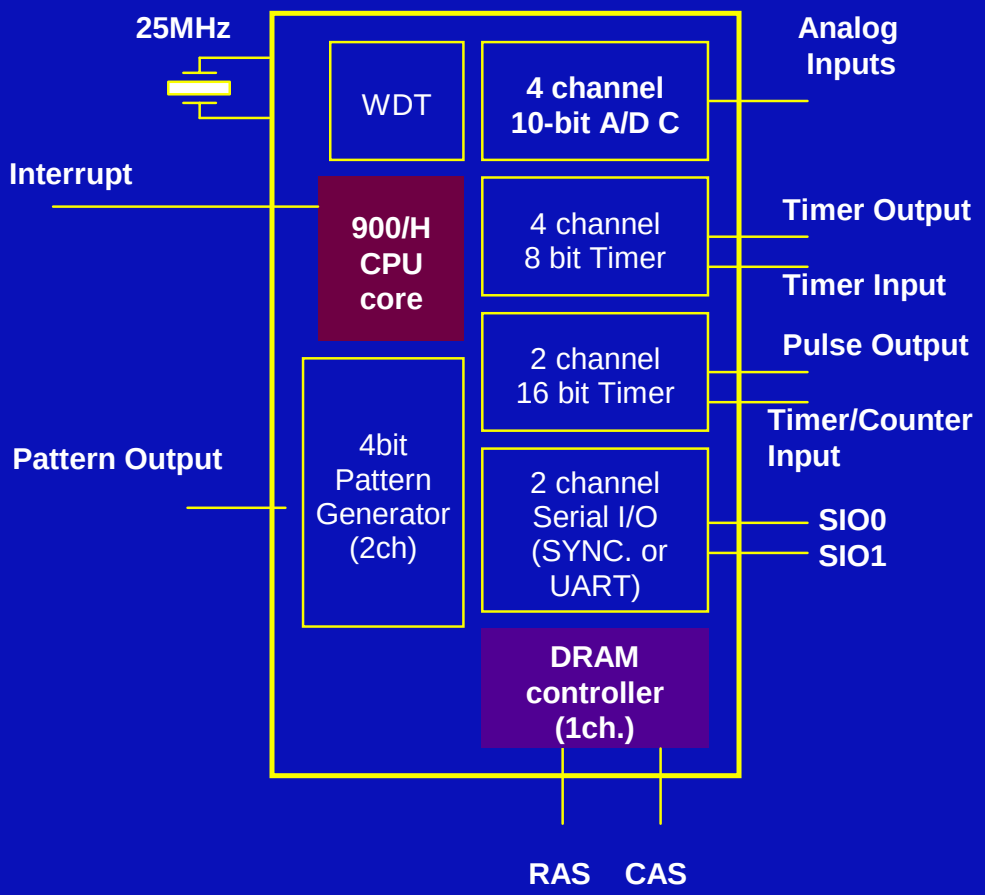
Type	ROM(byte)	RAM(byte)	
TMP93CS20F64K	4096	2048	
TMP93PW20AF		128K(OTP)	

TOSHIBA

TLCS-900

TMP95C061BF

- TLCS-900/H core
  - Min.Instruction Exec.Time=160ns(@25MHz)
- Easy Bus Interface
  - Separate bus (Address / Data)
  - DRAM Controller
- Memory Access Time
  - (@25MHz,0-WAIT)
    - ROM :100ns
    - DRAM: 70ns
- Package : 100pin QFP

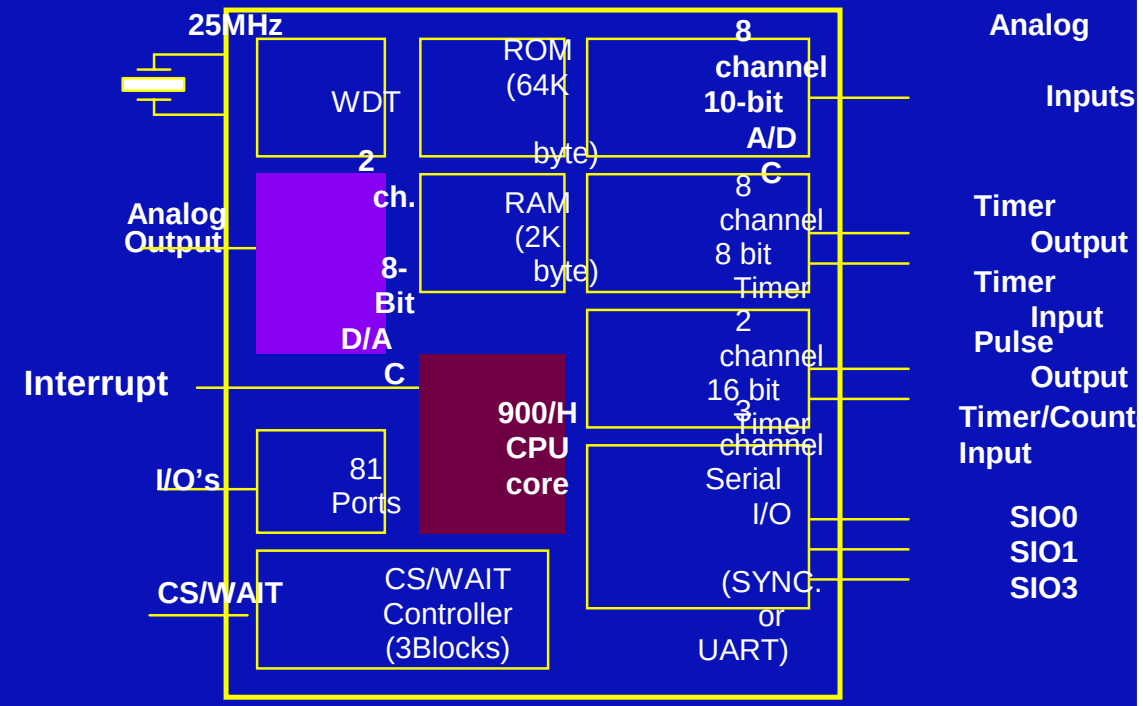


TOSHIBA

TLCS-900

TMP95Cx64F

- TLCS-900/H Core
- A/D converter : 10bit
  - External trigger
- 8 Bit D/A converter
- UART/SIO : 3 channel
  - Baud-rate clock input pin
- Package
  - 100 pin LQP



Memory variation

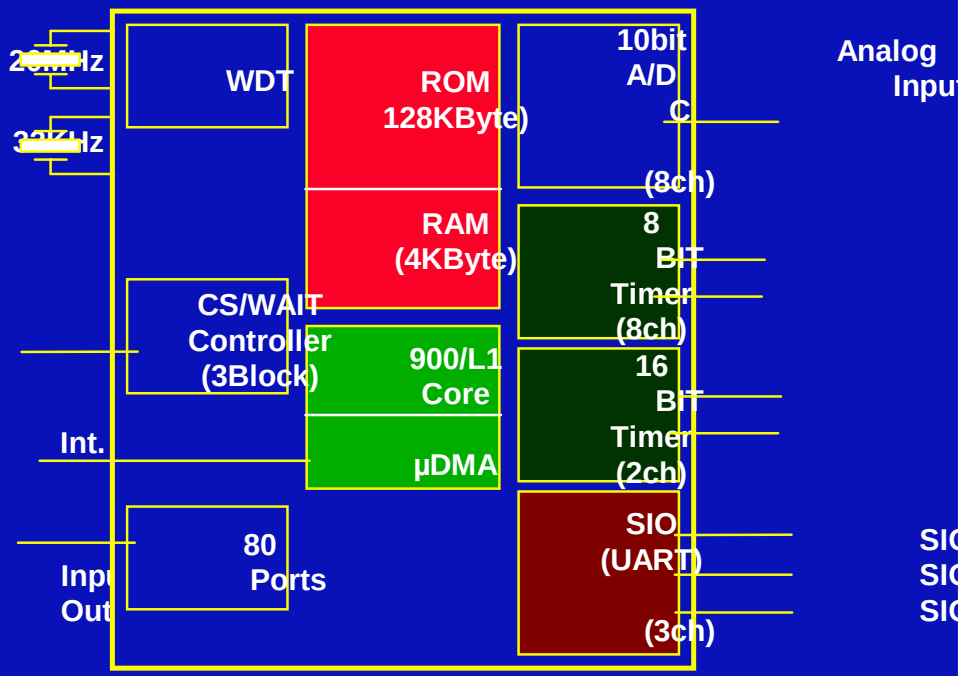
Type	ROM(byte)	RAM(byte)	
TMP95CS64F	64K	2K	
TMP95CW64F		128K	4K
TMP95PW64F	128K(OTP)		4K
TMP95FY64F	256K(FLASH)		8K
TMP95C265F	-	2K	

TOSHIBA

TLCS-900

TMP91CW10F

- TLCS-900/L1 core
  - Vcc = 2.7V, @16MHz
  - Vcc = 2.0V @10MHz
- A/D C : 10 bit x 8ch.
  - *20 usec (@2.7V, @25MHz)*
- Low Power Operation
  - Clock Gear
  - Dual Clock
  - 4 stand-by modes
- Package :
  - 100 pin LQFP



Memory variation

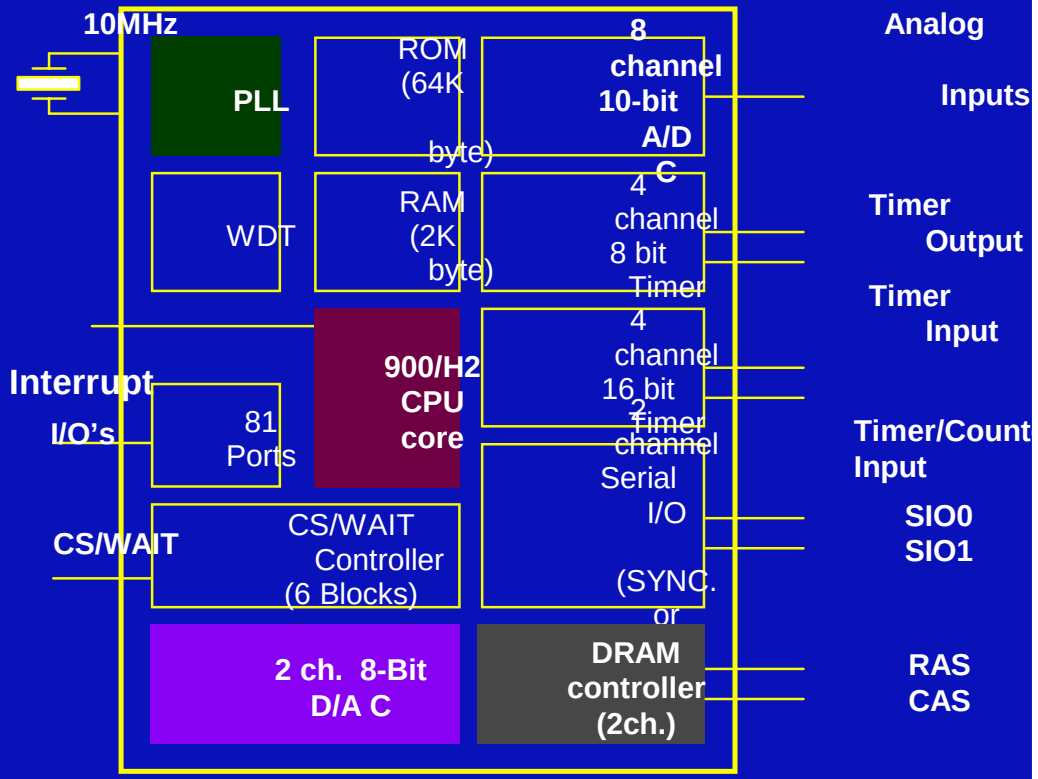
Type	ROM(byte)	RAM(byte)
TMP91CU10F	96K	3K
TMP91PW10F	128(OTP) 4K	

TOSHIBA

TLCS-900

TMP94C241BF

- TLCS-900/H2 core
  - 50ns (@20MHz)
- Dynamic Bus Sizing
  - 8/16/32bit bus
- µDMA
  - (8ch) : 300ns / 4 Byte
- PLL
  - Xin x4 internal clock
- Internal I/O
  - 2 ch. DRAM controller
  - 16bit Timer (4ch),
    - 8ch Capture
    - 8ch Compare
- Package
  - 160Pin-QFP
  - 144Pin QFP (ext. 16 Bit BUS)



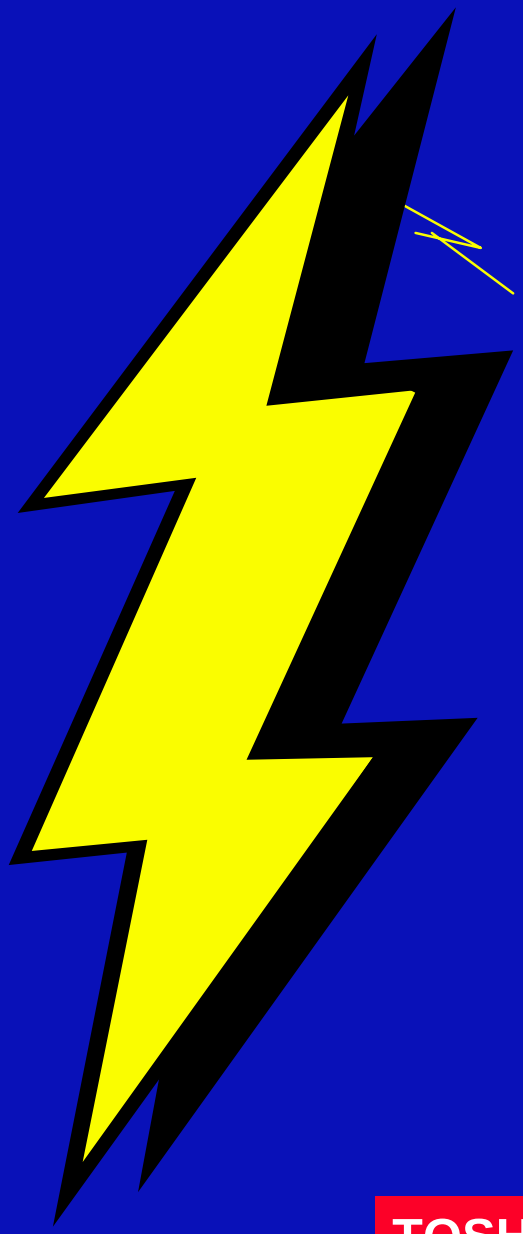
Memory variation

Type	ROM(byte)	RAM(byte)
TMP94C251F	-	2048
TMP94C241F	-	2048
TMP94CS40F**	64K	2048

TOSHIBA

TLCS-900

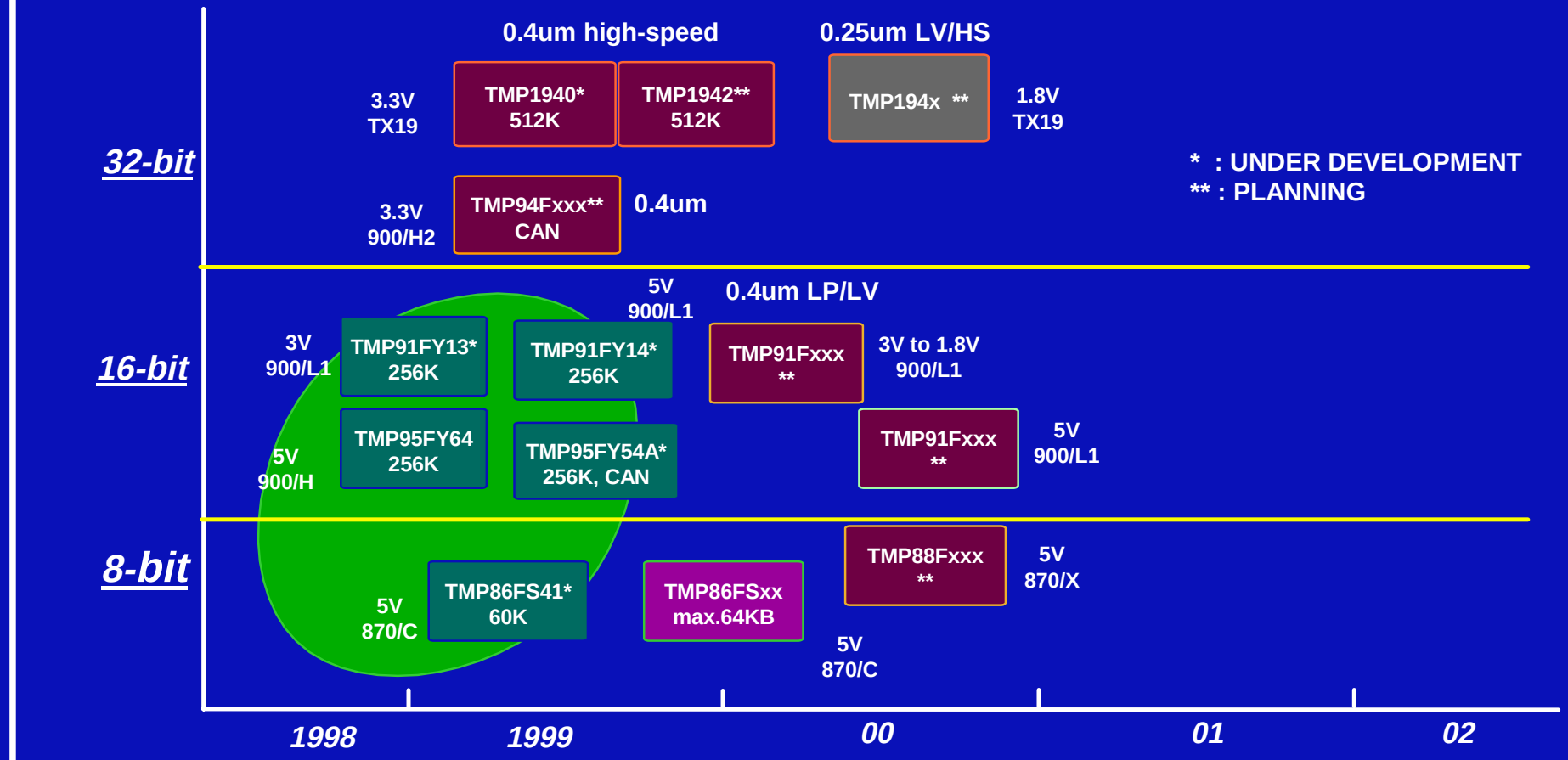
16-BIT MICROCONTROLLERS WITH FLASH MEMORY ON BOARD



TOSHIBA

TLCS-900

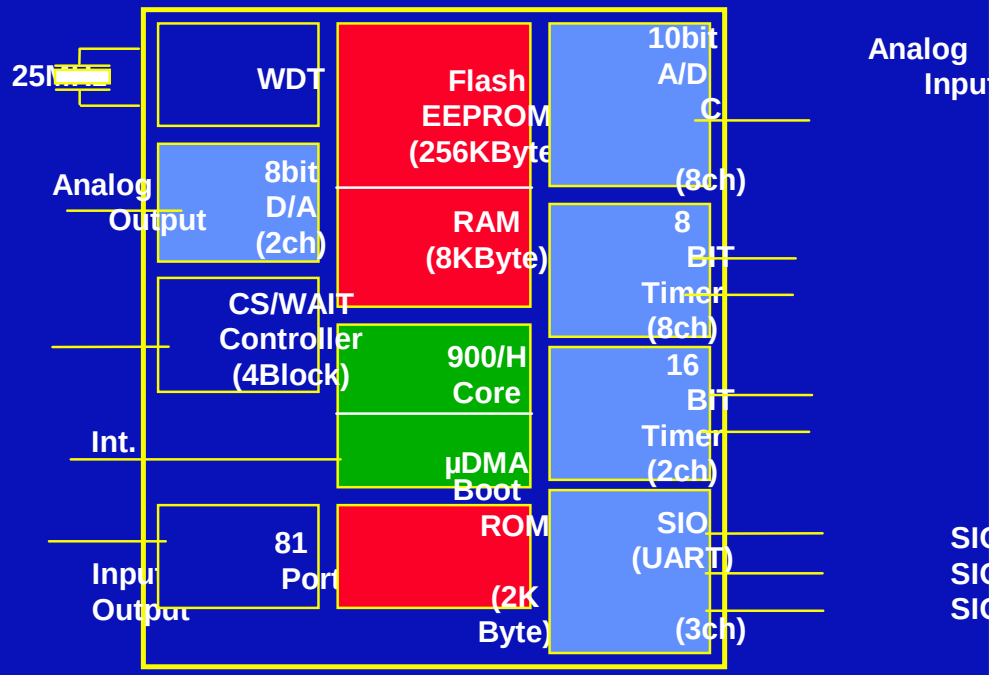
FLASH MCU ROAD MAP



TOSHIBA

TMP95FY64F

- TLCS-900/H core
- On chip Flash :
  - 256K (16K x 1, 8K x 2, 32K x 1, 64K x 3 Blocks)
- A/D C : *10 bit x 8 ch.*
  - *with external trigger*
- D/A Converter
  - *8 bit x 2 channel*
- SIO/UART x 3 ch.
  - *External Baudrate generator*
- Package :
  - 100 pin LQFP



Memory variation

Type	ROM(byte)	RAM(byte)
TMP95CS64F	64K	2K
TMP95CW64F	128K	4K
TMP95C265F	-	2K
TMP95PW64F	128K (OTP)	4K
TMP95FY64F	256(FLASH)	8K

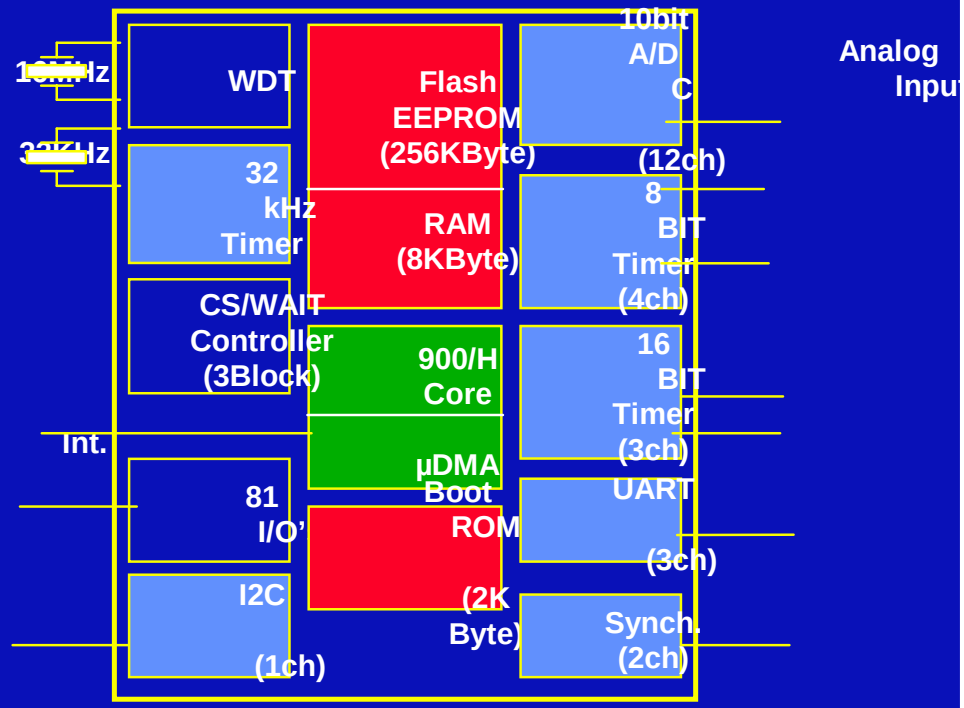
USP 4,382,279 owned by BULL CP8

TLCS-900

Under Development

TMP91FY13F

- TLCS-900/L1 core
  - 2.7 to 3.3 V operation
- On chip Flash, 3V :
  - 256K (16K x 1, 8K x 2, 32K x 1, 64K x 3 Blocks)
- A/D C : *10 bit x 12 ch.*
  - *with external trigger*
- 32 kHz Timer
- SIO
  - *UART x 3 ch.*
  - *Synch. x 2 ch.*
  - *I2C Bus x 1 ch.*
- Package :
  - 120 pin LQFP



Memory variation

Type	ROM(byte)	RAM(byte)
TMP91CY13F	256K	4K
TMP91FY13F	256(FLASH) 4K	

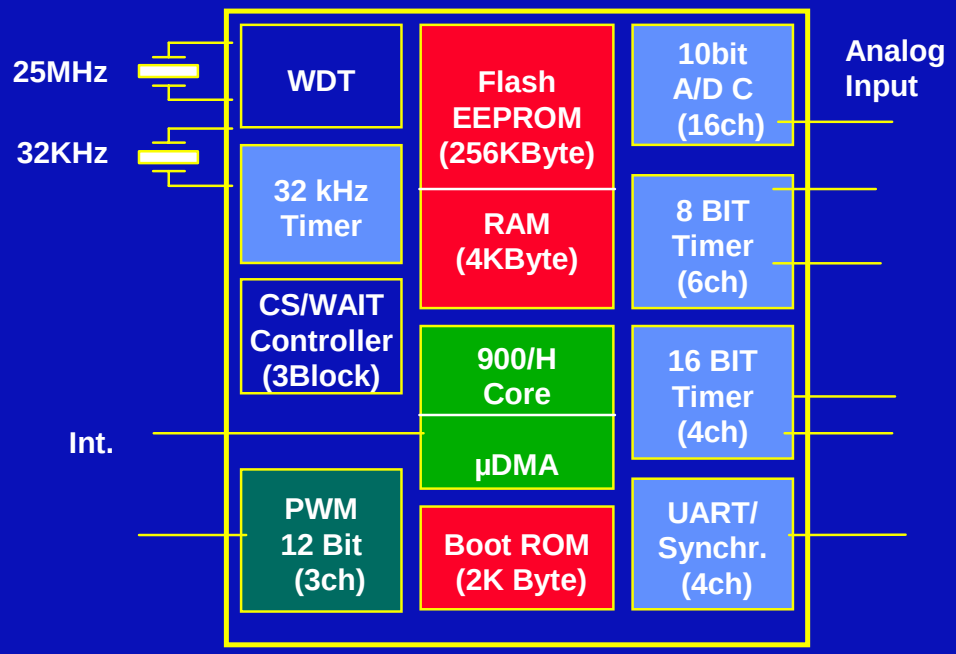
TOSHIBA

TLCS-900

TMP91FY14F

Under Development

- TLCS-900/L1 core
  - 5V operation
- On chip Flash :
  - 256K (16K x 1, 8K x 2, 32K x 1, 64K x 3 Blocks)
- ROM correction
- A/D C : *10 bit x 16 ch.*
  - *with external trigger*
- 32 kHz Timer
- PWM : 12 Bit x 3 ch.
- SIO
  - *UART/Synch. x 4 ch.*
- Package :
  - 100 pin LQFP



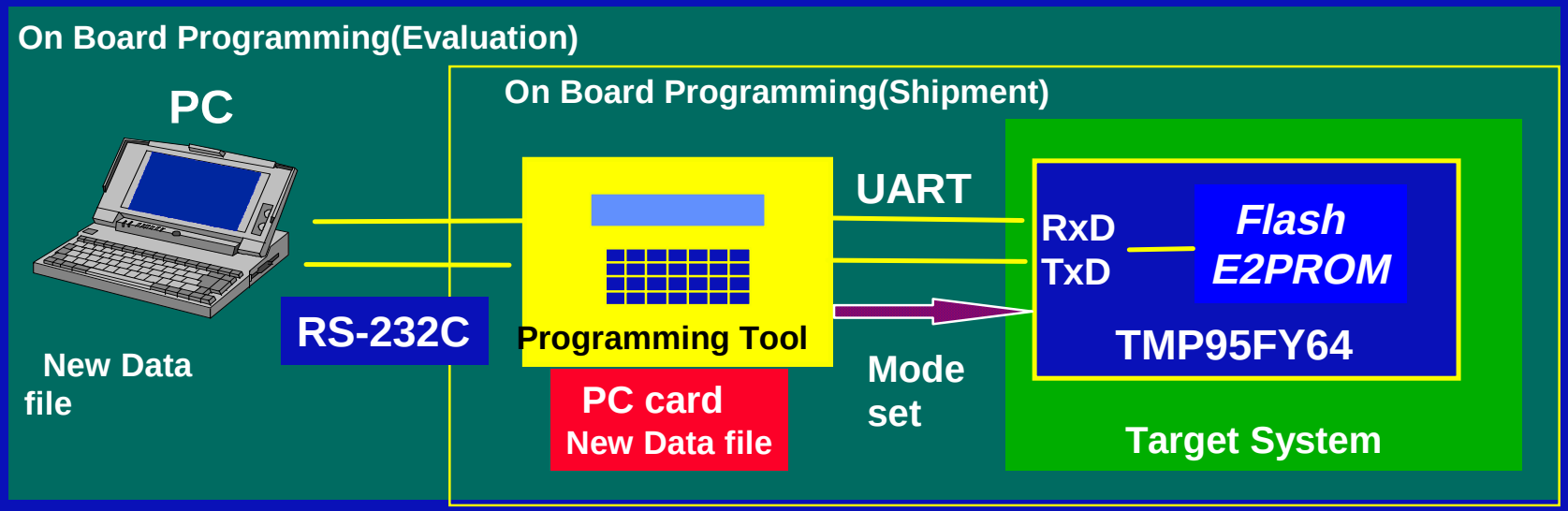
Memory variation

Type	ROM(byte)	RAM(byte)	
TMP91CW13F	128K	4K	
TMP91FY13F	256(FLASH)	4K	

TOSHIBA

ON BOARD PROGRAMMING

- ***3 types of Programming to support various process of development***
  - > *Trial* : Programming by EPROM Writer
    Prepare sockets for EPROM writer
  - > *Evaluation* : ON Board Programming by PC
    Easy Mode set using Programming Tool
  - > *Shipment* : ON Board Programming by Programming Tool
    Insert PC card with new data into Programming Tool



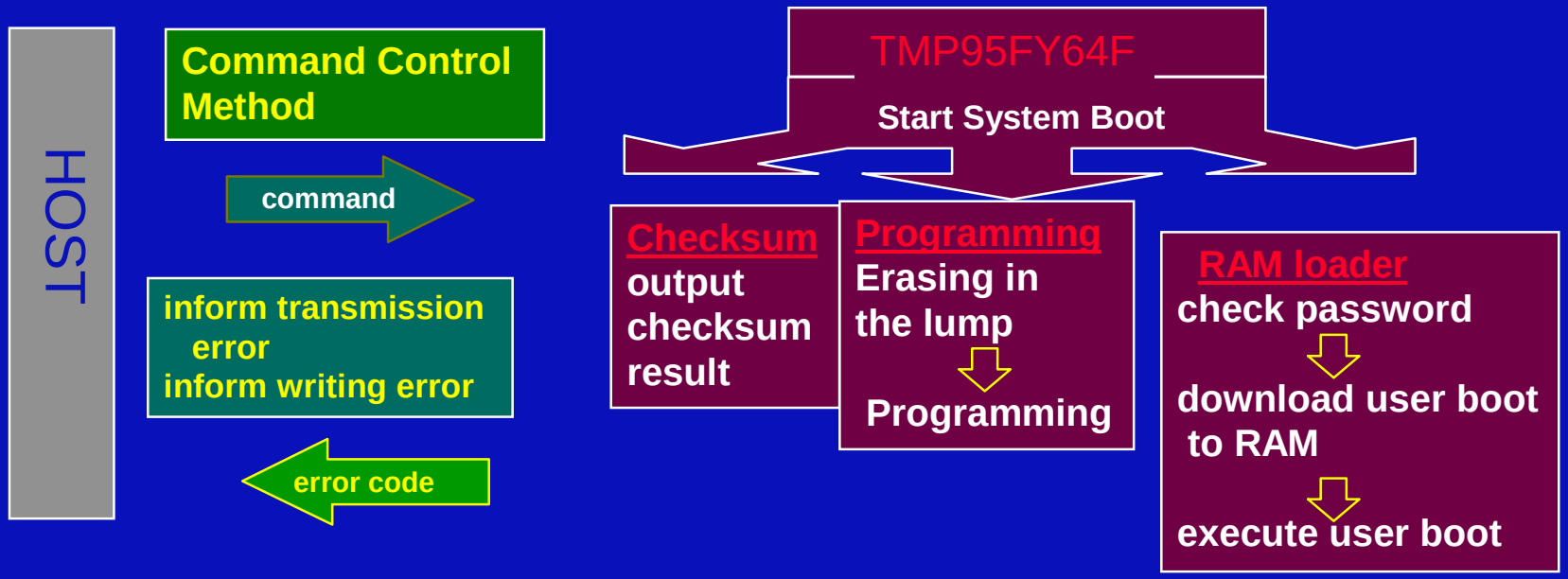
ON BOARD PROGRAMMING

- ***Boot Procedure suitable for on board programming***
- **Three Mode to support Effective Development of Software**

Checksum : Release Software engineer from complicated Past-record Management of Program

Programming in the lump : Can Reprogram efficiently using Erase in the lump

RAM Loader : Insure Security against illegal Reading and Cope flexibly with each user's Boot Sequence



On Chip TCAN Controller MCU

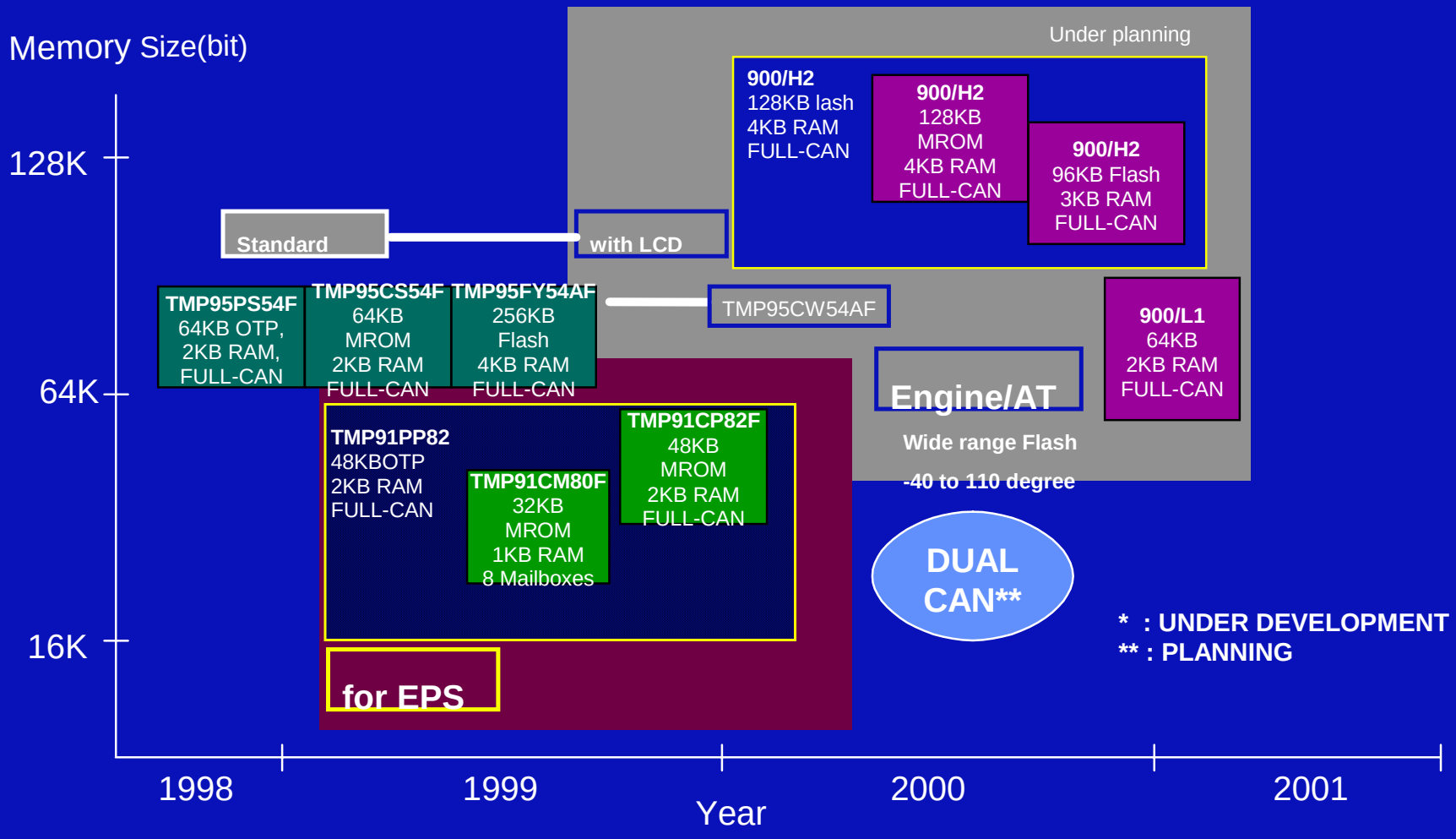
TCAN FEATURES

TCAN features short list

- 2.0B active
- Full-CAN Controller
- 16 Mailboxes (15 Receive&Transmit+1 Rec.-only)
- Baudrate up to 1MBit / s
- Extended Prescaler
- Bit Timing Parameter like AN82527
- Built in Time-Stamp Counter
- Readable Error Counters
- Warning Level IRQ, Error passive IRQ, Bus-off IRQ
- Local Loop Back Test Mode (Self Acknowledge)
- Built-in mechanism for internal Re-Arbitration
- Sleep Mode
- Wake-up on CAN-bus activity

TLCS-900

CAN MCU ROAD MAP



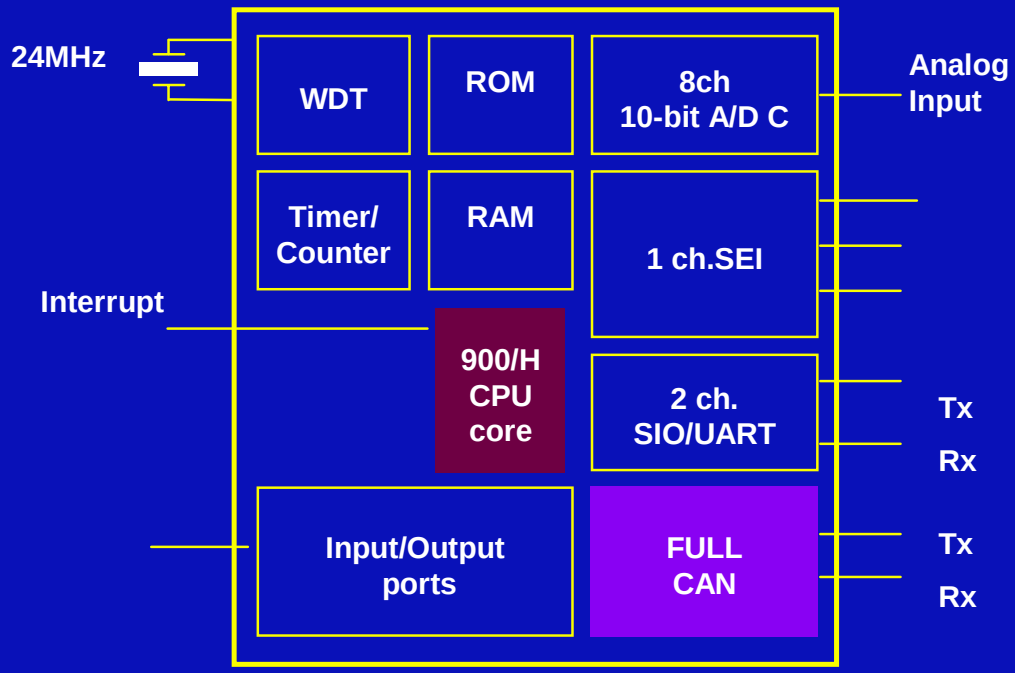
TOSHIBA

TLCS-900

TMP95CS54F

Under development

- TLCS-900/H core
- On chip Flash
- CAN
  - 2.0B, FULL CAN
  - 16 Mailboxes
  - Time stamp
- Internal I/O
  - 10 Bit A/D C x 8ch.
  - SIO/UART x 2 ch.
  - Timer (16Bit x2, 8Bit x8)
  - SEI x 1 ch.
- Package :
  - 100 pin LQFP



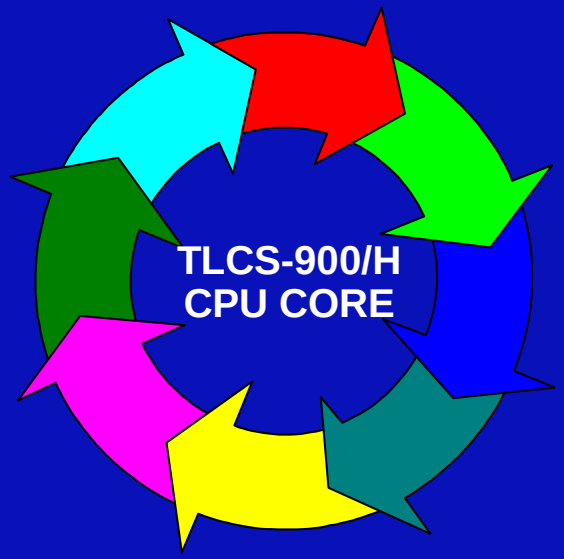
Memory variation

Type	ROM(byte)	RAM(byte)
TMP95CS54F	64K	2K
TMP95PS54F	64K (OTP)	2K
TMP95FY54AF	256K(FLASH)	4K

TLCS-900

The round picture

Pin and S/W compatible 16 Bit MCU´s



TMP95PW64F

The OTP

TMP95CS64F

The ROM

TMP95C265F

The ROM-less

TMP95FY64F

The FLASH

TMP95CS54F

The CAN

TMP95PS54F

The CAN OTP

*TMP95FY54AF

The CAN*

* UNDER DEVELOPMENT

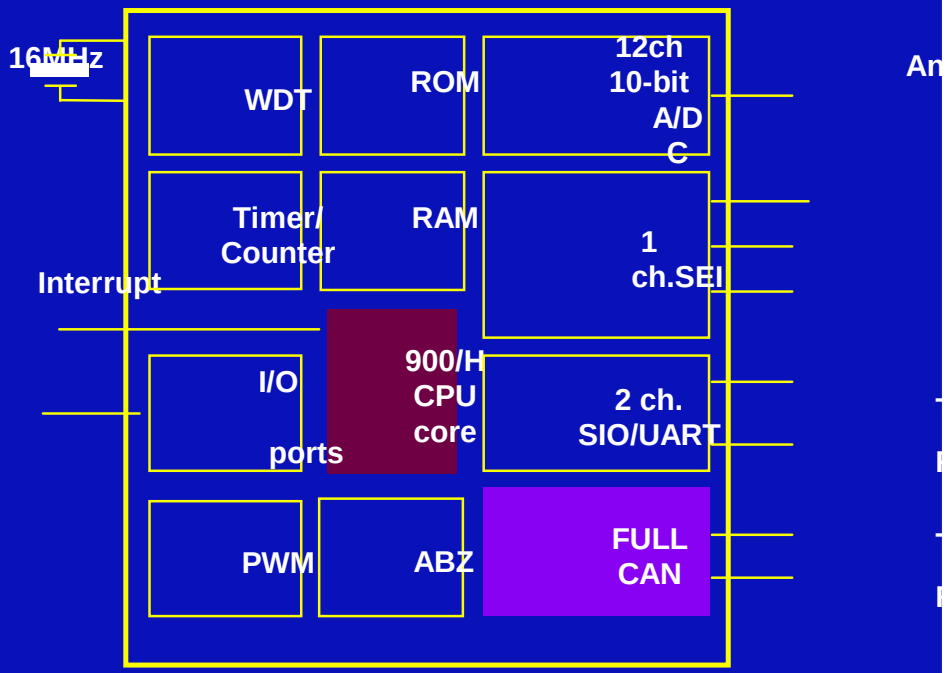
TOSHIBA

TLCS-900

TMP91CP8xF

Under development

- TLCS-900/L1 core, 5V
- CAN
  - 2.0B, FULL CAN
  - 16 (8) Mailboxes
  - Time stamp
- Internal I/O
  - *A/D C : 10 bit x 12 ch.*
  - *SIO/UART x 2 ch.*
  - *Timer (16Bit x2, 8Bit x4)*
  - *PWM : 16 Bit x 4 ch.*
  - *SEI x 1 ch.*
  - *ABZ phase measurement x 1ch.*
- Package :
  - 80 pin QFP
  - 100 pin QFP



Memory variation

Type	ROM(byte)	RAM(byte)
TMP91CP80F/CP82F	48 2K	
TMP91PP80F/PP82F	48K (OTP) 2K	

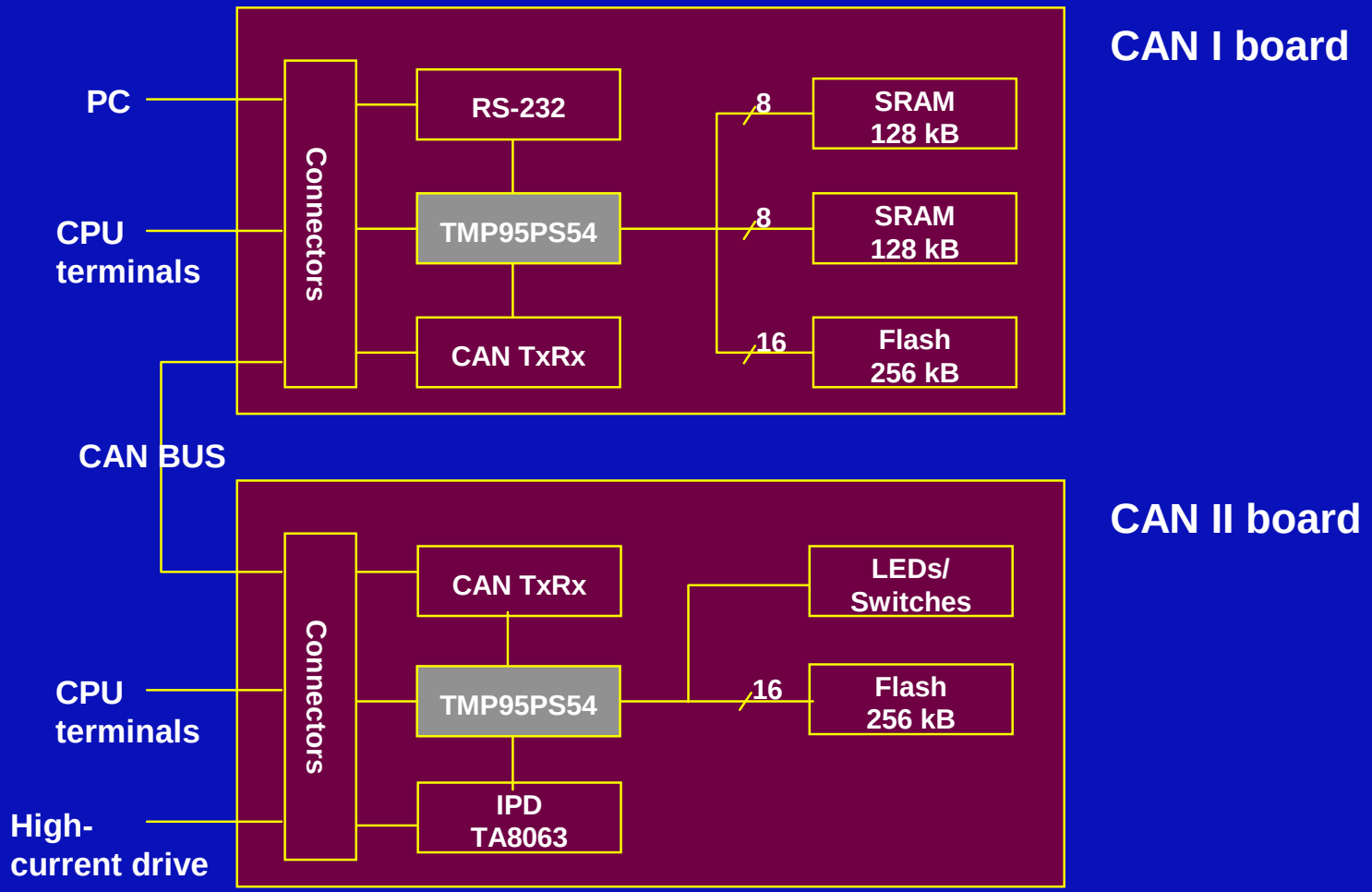
TOSHIBA

Starter-Kit TOPAS-900

- Features
  - Toshiba‘s **C compiler**, assembler, linker
  - Toshiba‘s Windows **UDE debugger**
  - Program development using high level language
  - Simple **program download** to the TLCS-900 board
  - C level program test with UDE debugger/ROM monitor
    - Single Step, Breakpoints, Symbolic Debugging
  - Easy switch to Toshiba emulator (RTE model 15/25)
- Supported MCU‘s
  - TLCS-900/L standard : TMP93CS41F
  - TLCS-900/H FLASH : TMP95FY64F
  - TLCS-900/H CAN : TMP95CS54F

TLCS-900

TOPAS900 CAN : Starter kit for CAN MCU



TOSHIBA